POWER SYSTEM HARMONIC MONITORING

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A thesis presented for the degree of Doctor of Philosophy
in Electrical and Electronic Engineering at the
University of Canterbury, Christchurch, New Zealand.

December 1992

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ABSTRACT

This thesis documents the design details, development, and field testing of an advanced power system harmonic monitor. It begins by reviewing present harmonic standards and harmonic monitoring equipment. It then goes on to describe the design and field use of the first generation harmonic monitor. From the field use a number of problems with this monitor are identified leading to the second generation harmonic monitor known as CHART II. The acronym CHART means Continuous Harmonic Analysis in Real-Time. The design of the monitor including the data acquisition and computer processing equipment, as well as the display system, is such that it can acquire multiple channels of power system signals from remote locations. It can compute the harmonics of these signals continuously, on a cycle-by-cycle basis, and store only the harmonics of interest. Harmonic computation is performed in real-time, with results displayed as they occur. Acquired data can be accurately time stamped for comparison with data from other monitoring sites, enabling simultaneous measurement at remote locations. The key areas of technology involved in implementing such an instrumentation system are: data acquisition from power system equipment, digital fibre optics, real-time digital signal processing, high speed multiprocessing bus systems, real-time multitasking operating systems, global positioning satellite systems, and computer networking. The application of digital signal processing to power system harmonic measurement is covered, and a field trial with the CHART II monitor is documented.

CONTENTS

PREFACE

This thesis presents the design theory and development of a very sophisticated harmonic monitor for use in policing harmonic legislation and for use as a research tool. The harmonic analysis instrumentation project was initiated by Professor Josu Arrillaga and Mr. Michael Dewe in 1986 in response to a request from the then New Zealand Electricity Division who defined the requirements for the monitor, and provided financial support.

I joined the research group working on the project at the end of 1988. At that stage a large amount of progress had been made on what is now known as the CHART I harmonic monitor, covered in Chapter 3, by the two primary researchers, Mr. Norman Hadfield and Mr. Alex Bould. Alex had developed the display system, while Norman had developed the harmonic analysis software and much of the Multibus II message passing software. In addition to this he had designed a six channel data acquisition system.

My initial intention was to complete the development of the monitor during 1989, after Norman and Alex had left, after which I would begin investigating its applications and actually using it in these applications. While Michael Dewe was on sabbatical during 1989, I worked under the supervision of Mr. Charles Lake and Professor Josu Arrillaga, completing the Multibus II software development and redesigning the digital end of the data acquisition system, including an integral component known as the *sample rate multiplier* with assistance from Mr. Peter Squires. Mr. Michael Cusdin designed and built an analog front end to the system, and Mr. Michael Shurety wrote the storage and compaction software to compact and store measured harmonic data.

By May 1990 a working prototype of the CHART I harmonic monitor was completed which was subsequently used in a field trial at the Islington substation in July 1990 in conjunction with Mr. Neil McKenzie of Design Power New Zealand Limited. This trial is discussed in Chapter 4. During this trial I realized that the harmonic monitor we had developed had a number of serious limitations, some of which are listed below:

- Clearly the monitor relies on its connection to the high voltage power system to obtain accurate information on the harmonic content of the currents and voltages, and yet must have sufficient isolation from the electromagnetic and electrostatic effects of the system. Our monitor had six analog inputs and relied on Design Power's fibre optical isolation system to transmit signals from voltage transformers and current transformers, located at remote sites in a high voltage switch yard. Although Design Power's fibre optical isolation is adequate for assessing compliance with New Zealand harmonic legislation, it was not adequate for the more thorough measurements that we required (because the instrumentation

associated with it could not resolve the fundamental component of a waveform).

- Our monitor was limited to six channels - expansion would require significant additional hardware and software development, including the addition of processing and data acquisition cards into the system.

- The display system had become outdated with the advent of standard windowing software such as Microsoft Windows. Because it was a custom design, it could only be upgraded or modified with a considerable programming effort by someone who was familiar with it.

In reality the harmonic monitor that we had developed was too limited to apply to research problems. In October 1990 I participated in the 7th International Conference of the Intel Real-Time Users Group (iRUG), presenting a paper covering the Multibus II software aspects of our system [3]. After discussions with people there involved with Multibus II, I became convinced that digital signal processors were the key to a successful harmonic monitoring system. At the same time Michael Dewe visited the 4th International Conference on Harmonics in Power Systems (ICHPS) to present a paper on the CHART I system [2]. There he held discussions with other researchers who were involved in developing harmonic monitoring systems, and making harmonic measurements. When I arrived back from the iRUG conference, and after meeting with Michael Dewe and Josu Arrillaga, I decided that rather than look at potential applications with our existing system, as I had originally intended to do, I would develop a new harmonic monitor providing that we could arrange the finance to do so. I designed a system level structure for the monitor, and Michael Dewe put a case to Transpower for funds for its development, who provided some 180 thousand dollars.

My work with the new monitor, now known as CHART II, accounts for the greater part of my original contribution to real-time harmonic monitoring of power systems. The design of the CHART II monitor is covered in Chapter 5, and has been published in the IEEE Power Engineering Society Transactions [4]. The structure of this system was designed by myself. The application of multirate digital signal processing techniques to harmonic measurement is covered in Chapter 6, and a paper on this was presented at the 1992 ICHPS conference [6], which has also been accepted for publication in the IEEE Power Engineering Society Transactions. This paper has so far been my major contribution in this field.

A working prototype of the CHART II harmonic monitor was completed in September 1992 in time for commissioning tests on the upgraded New Zealand inter Island HVdc link. These tests were performed at Benmore power station in October 1992, and at Haywards substation in November 1992, and are discussed in Chapter 7, with one of the tests covered in detail to illustrate a representative set of results from the CHART system. I intend to write a paper on these tests for submission to the 1993 IEEE Summer Power Meeting and for publication in the IEEE Power Engineering Society Transactions.

My work has lead to the completion of a very sophisticated harmonic monitor / data acquisition and processing system that can be used as a platform for investigating many areas of real-time harmonic measurement / power system transients. Some areas for future research with this system are: on-line harmonic analysis techniques used to detect and store only important harmonic data,

Expert Supervision of Convertor Operation in Real-Time where measured harmonic levels on a convertor are minimized by certain control techniques, and HVdc line and ac system fault location using CHARTs ability to precisely time stamp fault wavefronts at either end of a transmission line.

My contributions to the field of power system harmonic monitoring are summarized in the following list:

1. The design of a sophisticated harmonic monitoring system tailored to power systems. It can operate reliably in the very noisy environment of a high voltage switch yard.

2. Hardware and software design of a parallel processing system capable of continuous real-time data acquisition and processing of multiple channels.

3. The application of digital signal processing techniques to power system harmonic measurement.

4. The creation of a system with the capability of continuous on-line monitoring of harmonics and the investigation of a number of simple on-line analysis algorithms. The system is structured in such a way that other measurement techniques can be added. For example, other harmonic analysis techniques or even transient analysis techniques can be implemented.

5. The creation of a system with the ability to perform simultaneous time referenced measurements at remote locations.

The papers published as a result of my research are listed below in the order in which they were written. Copies of these papers are included in Appendix A which contains all papers and reports relating to the CHART project.

[1] A.J.V. Miller, C.B. Lake, M.R. Shurety and M.B. Dewe, "A six channel real-time harmonic monitor," *Proceedings of the 26th National Electronics Conference*, Wellington, New Zealand, September, 1989, pp. 121-126.

[2] C.B. Lake, M.B. Dewe and A.J.V. Miller, "Multichannel continuous real-time harmonic monitoring," *Proceedings of the 4th International Conference on Harmonic in Power Systems (ICHPS)*, Budapest, Hungary, October, 1990, pp. 424-430.

[3] A.J.V. Miller, C.B. Lake and M.B. Dewe, "Multichannel real-time harmonic analysis using the Intel Multibus II bus architecture," *Proceedings of the 7th Internaltional Conference of the Intel Real-Time Users Group (iRUG)*, St. Louis, Missouri, USA, October, 1990, pp. 11-24.

[4] A.J.V. Miller and M.B. Dewe, "Multichannel continuous harmonic analysis in real-time," *IEEE Transactions on Power Delivery*, Vol.7, No.4, October, 1992, pp. 1813-1819.

[5] A.J.V. Miller and M.B. Dewe, "Harmonic measurements on the New Zealand power system using CHART - a Continuous Harmonic Analyser in Real-Time," *Proceedings of the Institute of Professional Engineers New Zealand Annual Conference*, Christchurch, New Zealand, February, 1992, pp. 91-104.

[6] A.J.V. Miller and M.B. Dewe, "The application of multi-rate digital signal processing techniques to the measurement of power system harmonic levels," *Proceedings of the 5th IEEE International Conference on Harmonic in Power Systems (ICHPS)*, Atlanta, Georgia, September, 1990, pp. 7-15. Also accepted for publication in the IEEE Power Engineering Society Transactions.

Acknowledgements

In the development of the CHART I harmonic monitor I am grateful for the work of Michael Dewe, Norman Hadfield, and Alex Bould. I am also grateful for the assistance from Michael Cusdin and Michael Shurety, and in particular for the tremendous help during 1989 from Charles Lake who managed the project, and assisted me in programming Multibus II computers. I acknowledge the co-operation of the Electricity Corporation of New Zealand with the 1990 field trials, especially Neil McKenzie of Design Power New Zealand, and thank Michael Cusdin for his assistance.

In the development of the CHART II instrument I am indebted for the contribution from the following people: Michael Dewe who managed the project, Malcolm Barth for his help with the processor cards and discussion of technical ideas, Dermot Sallis for his help with data acquisition equipment and fibre optical links, and Dennis Chuah and Chen Shuin for their work on the PC display and networking software. I am very grateful for the tremendous assistance given to me by Dermot Sallis during the 1992 field trials, and thank Transpower New Zealand Ltd. for allowing us to make harmonic measurements on their system and to publish the results.

I thank my colleagues from the Power Systems Group for their help and interest in my project, namely S. Sankar, M. Zavahir, J.R. Camacho, A. Medina, J. de Souza, S. MacDonald, G. Anderson, Maria Luiza, Dr. C. Arnold, Dr. N. Watson, Dr. P.S. Bodger and especially Alan Wood (also for his many kayaking tips).

Throughout my research time working on the CHART project, Professor Josu Arrillaga has shown considerable interest, and I thank him for this as well as for the financial support from his research grant. I also thank Dr. Kumble Chandrashekar of TransPower New Zealand Ltd. for his interest in the project and for arranging the very generous financial support given by Transpower New Zealand Ltd. I acknowledge the award of a 1989 University Grants Committee postgraduate scholarship, a 1989 Christchurch Electricity Department postgraduate scholarship, and a 1990 Transpower postgraduate scholarship.

For his guidance and general project management I owe special thanks to my supervisor Michael Dewe. I also appreciate him presenting papers [4] and [6], allowing them to be published in the IEEE Power Engineering Society Transactions. I also thank Mr. Bill Kennedy for proof reading parts of my thesis, and for encouraging some of my other interests (eg. running and cycling) during my time as a postgraduate student.

Finally I thank my family, Patricia, John, Claire, and Elizabeth, for their support while I have been a student, especially Elizabeth for proof reading my thesis. Thanks also to my flatmates, and to Wendy for her special company.

GLOSSARY

Abbreviations and Acronyms

		Typical use
186/110A	A Micro Industries Multibus II prototyping computer	p. 24
486/133SE	The Intel 33MHz 80486 Multibus II computer	p. 40
8031	An Intel 8 bit micro-controller	p. 25
8086	An Intel 16 bit micro-processor	p. 18
80186	An Intel 16 bit micro-computer	p. 24
80286	An Intel 16 bit micro-processor	p. 26
80386	An Intel 32 bit micro-processor	p. 26
80486	An Intel 32 bit micro-processor	p. 47
8751	An Intel 8 bit micro-controller	p. 23
ac	Alternating Current	p. 34
ADC	Analog to Digital Convertor	p. 23
ALU	Arithmetic and Logic Unit	p. 43
AS	Australian Standard	p. 5
ASM86	An Intel 8086 micro-processor assembler	p. 26
BIST	Built In Self Test	p. 26
BMI	Basic Measuring Instruments	p. 14
BS	British Standard	p. 5
CCITT	International Consultive Committee on Telephone and Telegraphy	p. 6
CHART	Continuous Harmonic Analysis in Real-Time	p. 3
CPU	Central Processor Unit	p. 26
CT	Current Transformer	p. 29
CVT	Capacitor Voltage Transformer	p. 29
DAC	Digital to Analog Convertor	p. 16
DAPM	Data Acquisition and Processing Module	p. 39
dc	direct current	p. 1
DIT	Decimation In Time	p. 95

DFT	Discrete Fourier Transform	p. 2
DMA	Direct Memory Access	p. 25
DOS	Disk Operating System	p. 28
DRAM	Dynamic Random Access Memory	p. 25
DSM	Digital Services Module	p. 40
DSP	Digital Signal Processor	p. 3
EDI	Equivalent Disturbing Current	p. 7
EDV	Equivalent Disturbing Voltage	p. 6
EHV	Extra High Voltage	p. 17
EN	Enforcement Notification	p. 5
EPROM	Erasable Programmable Read Only Memory	p. 25
ESCORT	Expert Supervision of Convertor Operation in Real-Time	p. 122
Ethernet	A Standard 10 MEGA bit per second local area network	p. 37
FFT	Fast Fourier Transform	p. 3
FIFO	First In First Out	p. 23
FIR	Finite Impulse Response	p. 79
GPIB	General Purpose Interface Bus	p. 23
GPS	Global Positioning System	p. 37
HAIP	Harmonic Analysis Instrumentation Project	p. 21
HF	High Frequency	p. 1
HVdc	High Voltage direct current	p. 1
ICHPS	International Conference on Harmonics in Power Systems	p. 28
icon	A graphically drawn key	p. 27
IEC	International Electrotechnical Commission, U.S., Inc.	p. 5
IEEE	Institute of Electrical and Electronic Engineers	p. 6
I/O	Input/Output	p. 47
iRMX	Intel Real-Time Multitasking Operation System	p. 3
iRUG	Intel Real-Time Users Group	p. 28
iSBX	Intel System Bus eXtension - a Multibus II bus	p. 25
LAN	Local Area Network	p. 47
MIPS	Million Instructions Per Second	p. 91
MOD186	Additional support libraries for the 80186 micro-computer	p. 25
MPC	Message Passing Co-processor	p. 21
MSA	Multibus II Systems Architecture	p. 58
Multibus II	An advanced Intel multiprocessor bus architecture	p. 3
NZE	New Zealand Electricity	p. 2
NZED	New Zealand Electricity Division of the Ministry of Energy	p. 2

PC	Personal Computer	p. 13
PES	IEEE Power Engineering Society	p. 125
PL/M	Intel Programming Language M for 80x86 processors	p. 25
PSB	Parallel System Bus	p. 3
RAM	Random Access Memory	p. 15
RDCM	Remote Data Conversion Module	p. 38
RMS	Root Mean Square	p. 6
RS232	A Serial communication protocol	p. 17
RTC	Real-Time Clock	p. 49
SAFPSA	Selective Audio Frequency Power Spectrum Analyzer	p. 13
SBC	Single Board Computer	p. 24
SCADA	System Control And Data Acquisition	p. 37
SCSI	Small Computer Systems Interface	p. 47
SNR	Signal to Noise Ratio	p. 82
SRM	Sample Rate Multiplier	p. 23
TCP/IP	Transmission Control Protocol / Internet Protocol	p. 37
THD	Total Harmonic Distortion	p. 6
TMS320C26	A Texas Instruments 16 bit fixed point digital signal processor	p. 37
VT	Voltage Transformer	p. 29
Z-80	An 8 bit micro-processor	p. 17

Chapter 1

INTRODUCTION

Non-linear power electronic devices used in a power system to increase the efficiency of power supplies distort voltage and current waveforms from their ideal sinusoidal shape. Examples of these devices range from a small number of large schemes such as High Voltage direct current (HVdc) link convertors in the MEGA watt range, to medium power devices such as variable speed motor drives, electric traction, and arc furnaces, which are in the 100 kilo watt range, to many low power devices such as an office block equipped with many personal computers, fluorescent lighting, and uninterruptible power supplies, in the 100 watt region.

The effects of this distortion are varied and are usually detrimental. Some examples include audible interference with nearby telephone lines (such as a telephone line running parallel to a dc transmission line), capacitor bank failure due to increased heating by High Frequency (HF) signals, additional thermal losses in machines such as transformers, resulting in their possible destruction, and overloads in neutral conductors of three phase four wire distribution systems. Distorted voltage and current waveforms can also affect the operation of ripple control relays, and of critical power system protection relays, leading to unreliable operation of these devices.

Because distorted power system voltage and current waveforms are repetitive under steady state conditions, they can be represented by a Fourier series. This is the summation of a fundamental sinusoidal component with a series of higher order harmonic components at frequencies that are integer multiples of the fundamental frequency. Harmonic components are used extensively by power system engineers to quantify the distortion of voltage and current waveforms caused by non linearities in a network, which has lead to the idea of harmonic pollution on a network. Figure 1.1 shows the current waveform of a typical domestic washing machine with an electronic power supply and the harmonics produced by this.

Many countries that have experienced harmonic related problems have introduced standards or legislation that sets limits on harmonic levels. These standards and the terms they use are discussed in Chapter 2. Standards are clearly useless on their own - there must be some way of assessing compliance to them. Moreover, harmonic problems often only become apparent when equipment fails due to them. It is therefore important to identify these problems, before such catastrophic failures, by harmonic monitoring. The design, theory, and field use of a very sophisticated harmonic monitor for policing harmonic legislation and for advanced research is the topic of this Thesis.

Research on the monitor began in 1986 in response to a request from the then New Zealand

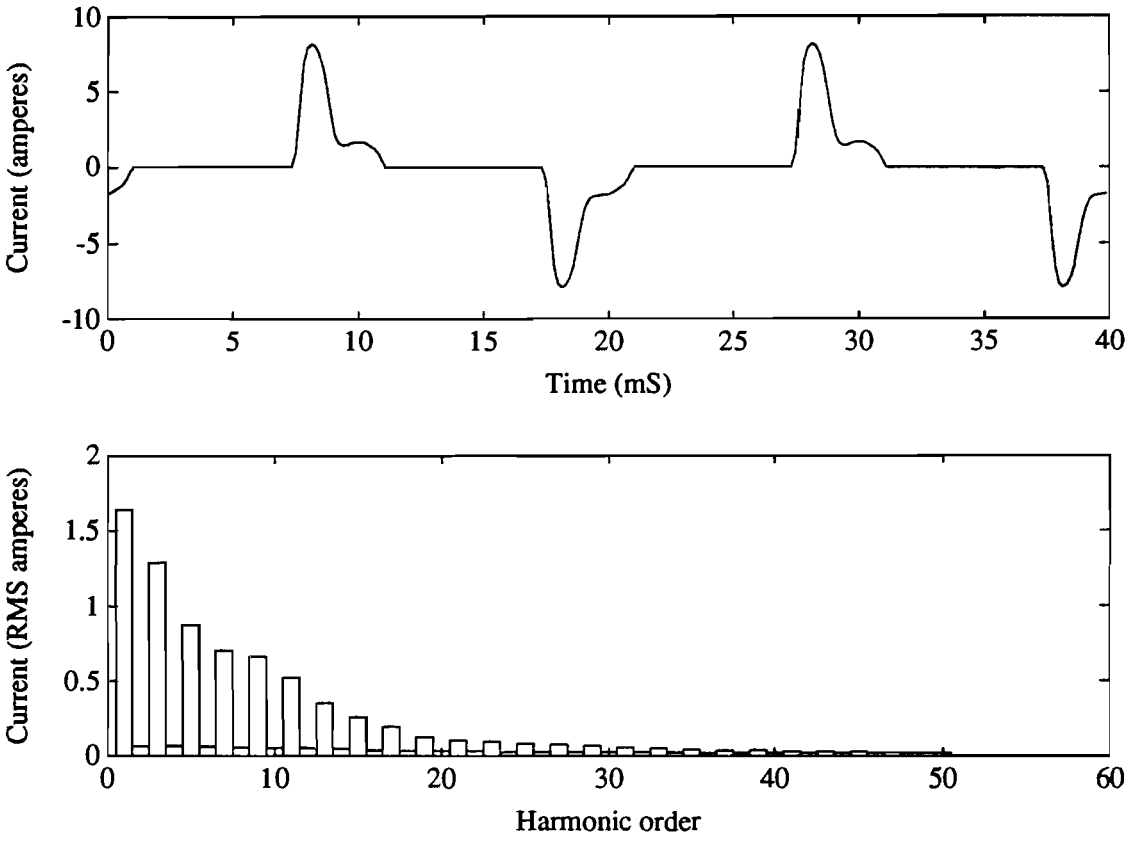


Figure 1.1 The current waveform harmonics produced by a domestic washing machine.

Electricity Division (NZED), who provided financial support and the requirements of the monitor [Goodwin, 1986]. These requirements encompassed the New Zealand legislation (reviewed in Section 2.2.3) and added the additional requirement of simultaneous measurement of all three phases of voltage and current. It also stated that digital computer equipment was preferred, and expressed a preference for equipment that would process as many cycles per minute as possible. These requirements were heavily based on the MAC-8 harmonic monitoring system discussed in Section 2.3.1.9, which was developed between 1975 and 1982 by the then New Zealand Electricity (NZE).

In 1986 the initial project team decided to design an instrument that would monitor each cycle of the fundamental waveform for six channels (3 voltages and 3 currents) continuously, computing the harmonics of each cycle in real-time to avoid the loss of data. This was in preference to a 'snapshot' approach where a number of cycles of data are captured and the harmonics of these are computed in non real-time. Harmonics are found from each cycle of sampled voltage or current waveforms by applying the Discrete Fourier Transform (DFT),

$$H(\frac{n}{NT}) = \sum_{k=0}^{N-1} h(kT)e^{\frac{-j2\pi nk}{N}}, \text{ for } n = 0, 1, \cdots, N-1 \tag{1.1}$$

over an integer multiple of fundamental periods, illustrated in Figure 1.2. The DFT is an approx-

imation to the continuous Fourier transform, and is computed using an efficient algorithm known as the Fast Fourier Transform (FFT).

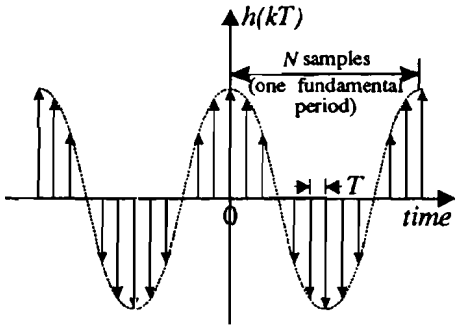


Figure 1.2 The discrete Fourier transform is taken over an integer number of fundamental periods of a voltage or current waveform (one period in this example).

The continuous harmonic analysis approach adopted at the beginning of the project lead to the acronym **CHART**, which means *Continuous Harmonic Analysis in Real-Time.* To match the processing and data throughput demands of such an approach, the advanced bus architecture Multibus II was chosen as the base of the instrument, in conjunction with Intel's *real-time multitasking* operating system, iRMX. This instrument (now known as CHART I) is discussed in Chapter 3.

A successful prototype of the CHART I harmonic monitor was completed in 1990, and was used in the same year to make harmonic measurements on the New Zealand South Island power system at the Islington substation in conjunction with Design Power New Zealand Ltd. This is discussed in Chapter 4.

The 1990 field trials highlighted a number of problems with CHART I, and after visits to international conferences and discussions with people involved in similar areas of technology by the author and Mr. M.B. Dewe, a significant change to CHART I was conceived, leading to the superior CHART II system discussed in Chapter 5. It was concluded at that time that Digital Signal Processor (DSP) technology was a very sound way of meeting the processing requirements of a multiple channel monitor. However a decision to use DSPs raised an important issue concerning the bus system used by CHART II. If Multibus II was to be kept as the bus standard in the instrument, it was necessary to develop a DSP board with a full Multibus II interface, as there were no commercially available Multibus II DSP boards capable of meeting the requirements of CHART at that time. Alternatively a different bus system such as VME, EISA, or Microchannel for which DSP boards are available could be adopted.

Eventually a decision to continue with Multibus II was made, building on our expertise with Multibus II, Multibus II computer design, and the iRMX operating system. This decision was also influenced by the availability of Multibus II prototyping boards from Microindustries of the USA. These are essentially complete interfaces to the Multibus II Parallel System Bus (PSB) and incorporate the Intel 80186 micro-computer, giving an intelligent interface, while leaving over half of the board area free for prototyping designs. These boards have been used as the Multibus II interface for DSP boards developed as part of the CHART project. The DSP boards themselves

interface to the 80186 processor bus and control signals available on the prototyping board.

With the tremendous processing power afforded by one DSP per channel in CHART II, more advanced processing algorithms were used to simplify data acquisition hardware and to improve the acquired signal quality. These processing algorithms are discussed in Chapter 6, together with the fundamentals of data acquisition and sampling for the Fast Fourier Transform.

In September 1992 a working prototype of a 10 channel CHART II system was completed. This was subsequently used in field trials during commissioning tests on the upgraded New Zealand HVdc link in October and November 1992. These trials and the harmonic measurements made during them are covered in Chapter 7. To illustrate a range of parameters that CHART II can monitor and compute, a representative sample of results is included in Chapter 7.

The thesis is concluded in Chapter 8 with a summary of CHART II's features, a review of its history, and a discussion of future work to be conducted using CHART II.

Chapter 2

HARMONIC STANDARDS AND MONITORING EQUIPMENT

2.1 Introduction

Many European countries as well as the United States, Australia, and New Zealand have published standards limiting harmonic current and voltage levels on their power systems. In addition to setting limits, these standards also set out requirements for harmonic monitoring instrumentation, as it would be impossible to assess compliance with harmonic standards without such equipment. This chapter discusses harmonic standards by firstly defining a number of terms and assessment criteria for harmonic levels and discussing criteria for assessing harmonic interference in communication circuits. It then discusses harmonic standards, summarizing New Zealand's harmonic legislation, and the Australian Standard AS 2279 which is based on the United Kingdom recommendation from which many other standards have been derived. Finally it reviews a number of harmonic monitors, developed both commercially and through research for assessing compliance to standards, or for research purposes.

2.2 Harmonic Standards

Standards limiting the harmonic production of loads account for the various types of loads in two categories. The first category is characterized by domestic loads, where the total load is formed by the connection of a large number of small consumers to the system. Standards limiting harmonic currents generated by domestic appliances first appeared in the European standard EN 50 006 of 1976 and in IEC 555. The standard EN 50 006 was adopted in various forms by countries such as West Germany as the DIN EN 50 006 / VDE 0838 [Glerse, 1992], the United Kingdom as BS 5406 [BSI, 1988] and Australia as part 1 of AS 2279-1991. A revision of the IEC 555 standard has lead to the publication of the new EN 60 555 standard, which replaces EN 50 006, and the publication of a new IEC 555 standard.

Other standards limiting harmonic currents or harmonic voltage distortion for individual supply system voltages at the point of common coupling deal with the second category of loads - the industrial consumers. Engineering recommendation G5/3 for the United Kingdom is an example of this, and is effectively an electricity supply authorities document. Australian standards have combined this with BS 5406 to produce a two part document covering both domestic

and industrial type equipment in AS 2279 [Baitch, 1982], updated in 1991. In the United States, the Institute of Electrical and Electronic Engineers (IEEE) *"Recommended Practices and Requirements for Harmonic Control in Electric Power Systems"* (project IEEE-519, 1991) sets limits for the percentage total harmonic distortion, as well as harmonic current limits for general transmission distribution systems (between 120 V and 69 kV), general subtransmission systems (69 kV to 161 kV), and high voltage systems (over 161 kV). Other countries including the USSR [Järvik, 1990], France and Sweden [Arrillaga *et al.*, 1985a], Finland, Holland, and Switzerland [de Oliveira *et al.*, 1992] have also adopted harmonic standards which generally set limits on individual harmonic voltage and total harmonic voltage distortion for various system voltages relating to distribution and transmission systems. New Zealand has introduced harmonic legislation in the *"Limitation of Harmonic Levels Notice 1983"*, which is discussed in Section 2.2.3. As an example of a standard based on the Engineering Recommendation G5/3 for the United Kingdom (on which many other standards are based), the Australian standard AS 2279 part 2 is discussed in Section 2.2.4. While the standards of these two countries have been reviewed, no comparisons between them have been made, as each one has been developed to meet the needs of a specific electrical power system. In addition to setting harmonic limits, the standards set out requirements for harmonic monitoring equipment, which are summarized for New Zealand legislation in Section 2.2.3 and for the Australian standard in Section 2.2.4.

2.2.1 Definition of Terms

Individual harmonic voltage is given by

$$U_n = 100\frac{E_n}{E_1}\%, \tag{2.1}$$

where E_n is the phase-to-earth Root Mean Square (RMS) voltage of harmonic order n, and E_1 is the phase-to-earth RMS fundamental frequency voltage, except in the case of New Zealand legislation where

$$U_n = 100\frac{E_n}{E_{ph}}\%, \tag{2.2}$$

in which E_{ph} is the RMS nominal system phase-to-earth voltage. This is elaborated on in Section 2.2.3.

The Total Harmonic voltage Distortion (THD) is given by

$$U_t = \sqrt{\sum_{n=2}^{50} U_n^2}\%, \tag{2.3}$$

and the Equivalent Disturbing Voltage (EDV), as defined in [CCITT, 1989] and [NZED, 1983], is given by

$$EDV = 6.25 \times 10^{-5}\sqrt{\sum_{n=2}^{50} (nP_nU_n)^2}\%, \tag{2.4}$$

where P_n is the psophometric weighting given to frequency $50n$ in the psophometric weighting table, set out in [CCITT, 1989] and [NZED, 1983].

Individual harmonic current (I_n) is the RMS current in amperes of harmonic of order n flowing between any consumer and that consumer's point of common coupling and is always specified in amperes. Equivalent Disturbing Durrent (EDI) is given by

$$EDI = 6.25 \times 10^{-5} \sqrt{\sum_{n=2}^{50} (nP_nI_n)^2} \text{ amperes,} \tag{2.5}$$

defined in [CCITT, 1989] and [NZED, 1983].

2.2.2 Harmonic Interference in Communication Circuits

As discussed in Chapter 1, harmonics can cause interference in communication circuits by inducing audible currents in them. This interference is a function of the coupling between the power and communication circuits and the frequency response of the telephone receiver/human ear combination. For studies of noise interference, the excessive quantity of data containing the spectrum of harmonics in the disturbing current can be reduced significantly by using the psophometrically-weighted current, defined by Equation 2.5. The psophometric weighting tables are designed to account for the coupling between the power and communication circuits and for the frequency response of the telephone receiver/human ear combination. Although psophometric weighting is known to be inaccurate [CCITT, 1989], it is widely used as a measure of compliance with harmonic standards. However, with changing communication apparatus, psophometric weighting is becoming increasingly out-dated - a communication modem for instance has a different frequency response than that of the telephone receiver/human ear combination and is consequently affected by different harmonics.

Unbalances in a power system will cause residual harmonic currents to flow. It is these currents that will induce noise in communication circuits, and the psophometrically-weighted current should therefore be calculated from the residual current (the vector sum of all three phases, which requires harmonic phase information as well as magnitude). Because of the uncertainty that exists in harmonic standards and legislation, EDI is usually calculated for each individual phase, rather than calculating the psophometrically-weighted residual current. Research has shown however [Kuussaari and Pesonen, 1976], that EDI calculated from the balanced line current is always higher than the psophometrically-weighted residual current. It is therefore feasible to calculate EDI from the balanced line current, and if this is below the recommended limit, it is highly likely that interference from any residual current will be minimal. However this approach is pessimistic and may often result in more expensive harmonic filters at a convertor station. From a commercial perspective this may be unacceptable, highlighting the need for measurement of residual current.

2.2.3 New Zealand Harmonic Legislation

New Zealand harmonic legislation has been derived by considering the experience of the Electricity Division, and is given in the *"Limitation of Harmonic Levels Notice 1983"*, which was gazetted in December 1981, came into force in December 1982, and was re-issued in 1983 [NZED, 1983]. Limits in the Notice were also derived with reference to the following recommendations/standards:

- Electricity Council Engineering Recommendation G 5/3, "Limits for Harmonics in the United Kingdom Electricity Supply System",
- British Standard BS 5406: 1976 (Cenelec EN50.006) "The Limitation of Disturbances in Electricity Supply Networks Caused by Domestic and Similar Appliances Equipped With Electronic Devices".
- Australian Standard AS2279, Parts 1 and 2: 1979 "Disturbances in Mains Supply Networks".

The Notice sets limits for harmonic voltage and current on the New Zealand public electricity supply network at all voltage levels down to and including 400/230 volts, specifically excluding signals introduced onto the system for load control, and can be divided into the following three sections. Supporting documents giving guidance on the application of the Notice are published with the Notice. New Zealand legislation has been controlled by the capabilities of the harmonic monitoring instrumentation available at the time it was written - namely the MAC-8 system used by the then New Zealand Electricity. An example of this 'controlling of legislation' is the modified definition of individual voltage harmonic distortion given by Equation 2.2. In this equation voltage harmonics are scaled by the nominal system voltage rather than the fundamental voltage of the strictly correct Equation 2.1. This is because the MAC-8 system cannot compute the fundamental voltage, as it is preceded by very steep high pass filters that attenuate the fundamental (discussed in Section 4.2.1).

2.2.3.1 Transmission System Limits

This section of the Notice covers harmonic levels on systems of 66 kV and above, which is the transmission system. Table 2.1 lists the maximum permitted harmonic voltage levels at any point of common coupling in the transmission system[1]. A limit of 1% is set on the EDV given by equation 2.4, and no limit is specified for total harmonic distortion. The limits on the harmonic current that may flow between a consumer and that consumer's point of common coupling are given in Table 2.2. The EDI limits are set out in Table 2.3.

Transmission system limits are based on the establishment of levels of harmonic voltage which are acceptable both in terms of the level of interference and the cost of controlling the harmonics. Amplitudes of harmonics produced by the majority of nonlinear loads tend to vary inversely with frequency, as does the cost of introducing harmonic filtering, while the susceptibility of

[1]The point of common coupling is that busbar electrically closest to any consumer through which any current must flow to that consumer and one or more other consumers.

Harmonic order n	Harmonic voltage limit, U_n (phase to earth harmonic voltage expressed as a percentage of the nominal phase to earth system voltage).
3	2.3
5	1.4
7	1.0
9	0.8
11	0.7
13	0.6
15	0.5
17 to 21	0.4
23 to 49	0.3
Harmonic order n	Harmonic voltage limit, U_n (phase to earth harmonic voltage expressed as a percentage of the nominal phase to earth system voltage).
2	1.2
4	0.6
6	0.4
8 and 10	0.3
12 to 50	0.2

Table 2.1 New Zealand transmission system harmonic voltage limits.

communication circuits to interference increases with frequency. These factors, together with observed levels of odd and even harmonics, influenced the choice of the levels.

After the establishment of harmonic voltage limits, allowable harmonic current limits at the point of common coupling were determined such that the allowable harmonic voltage was not exceeded on other parts of the system. These current limits were determined by considering standing waves on transmission lines that cause the amplification of harmonic voltages and currents at remote points - a situation that has arisen in New Zealand. The worst case scenario was considered, where a voltage minimum on a transmission line due to a standing wave occurs at a point of common coupling, and the related voltage maximum occurs a quarter of a wavelength away. This leads to a current maximum, defined in terms of the maximum voltage divided by the lines characteristic impedance. Voltage and current limits along with their detailed derivations are given in [NZED, 1983] and [Bradley *et al.*, 1985b].

Harmonic order n	Harmonic current limit, I_n (RMS amperes at nominal system voltage).		
	220 kV	110 kV	66 kV
3	5.7	2.9	1.7
5	3.4	1.7	1.1
7	2.5	1.3	0.8
9	1.9	1.0	0.6
11	1.6	0.8	0.5
13	1.4	0.7	0.4
15	1.2	0.6	0.4
17	1.0	0.5	0.3
19 and 21	0.9	0.5	0.3
23	0.8	0.4	0.3
25 to 49	0.7	0.4	0.3

Harmonic order n	Harmonic current limit, I_n (RMS amperes at nominal system voltage).		
	220 kV	110 kV	66 kV
2	2.9	1.5	0.9
4	1.5	0.8	0.5
6	1.0	0.5	0.3
8	0.8	0.4	0.3
10	0.6	0.3	0.2
12 and 14	0.5	0.3	0.2
16 and 18	0.4	0.2	0.2
20 to 50	0.3	0.2	0.2

Table 2.2 New Zealand transmission system harmonic current limits.

2.2.3.2 Distribution System Limits

This section covers permitted harmonic levels on systems below 66 kV which is the distribution system. Distribution system limits are defined in terms of permitted levels of harmonic voltage distortion. They are 4% of any odd harmonic, and 2% of any even harmonic. A limit of 5% is placed on the THD given by Equation 2.3, using Equation 2.2 for harmonic voltage distortion.

Nominal system voltage (kV)	EDI (RMS amperes)
66	0.8
110	1.3
220	2.6

Table 2.3 New Zealand transmission system Equivalent Disturbing Current (EDI) limit.

2.2.3.3 The Measurement Schedule

The Notice specifies the requirements of harmonic measuring systems for assessing compliance with its conditions, which are summarized below. It allows either analog or digital instruments to be used, although the measurement schedule was written around the MAC-8 system discussed in Section 2.3.1.9.

(a) The error in measuring a constant harmonic voltage shall not exceed 0.1% of the nominal phase to earth system voltage.

(b) The error in measuring a constant harmonic current shall not exceed 0.2 A.

(c) The selectivity of the measuring system shall be such that a signal with a 50 Hz separation from that being measured shall have a minimum attenuation of 40 dB.

(d) The Measuring system shall either have a measurement time constant of between 0.08 s and 0.12 s, inclusive, or shall average the input over 4, 5 or 6 cycles of the actual system frequency.

(e) When a constant harmonic signal in the range 100-2500 Hz is applied to the measuring system, the maximum indication by overshoot shall not exceed the steady state indication by more than 5%.

The Notice also requires that harmonic measuring instruments find up to the 50th harmonic, and states that harmonic monitoring is to be performed when the system frequency is between the limits of 49.75 Hz and 50.25 Hz.

2.2.4 The Australian Standard - AS2279-1991

Part 1 of the Australian standard AS 2279 deals with the limitation of harmonics caused by household and similar electrical appliances. Part 2 deals with the limitation of harmonic levels caused by industrial equipment [Baitch, 1982]. It is classified into three stages according to the size of equipment under consideration, and covers transmission and distribution systems, specifying voltage distortion limits for each system. These limits are set out in Table 2.4. The standard

Supply system	Voltage at the point of common coupling (kV)	Total harmonic voltage distortion (%)	Individual harmonic voltage (%)	
			Odd	Even
Primary and secondary distribution	≤ 33	5	4	2
Transmission and sub transmission	22,33, and 66	3	2	1
	≥ 110	1.5	1	0.5

Table 2.4 Harmonic voltage limits at any point on the Australian system (including background limits).

allows harmonic producing loads that only operate in short bursts, and gives flow diagrams for the standards implementation.

Part 2 of the standard gives no information on how harmonic voltages are to be measured or what type of instrumentation should be used, stating that this is still under consideration. Part 1 however specifies that virtually any type of analyzer can be used (including the analog selective filter type, spectrum analyzers, and DFT analyzers). The analyzer requirements of AS 2279 part 1 are set out below.

(a) The error in measuring current shall not exceed the greater of 5% of the permissible limit or 0.015 A.

(b) The input selectivity should be such that an adjacent harmonic should have and attenuation of greater than 50 dB.

(c) The indicating/recording output response (applicable to analog monitors) should be that of a first order low pass filter with a time constant of 1.5 s (±10%).

(d) The bandwidth of each harmonic output should be between 3 Hz and 10 Hz.

(e) DFT analyzers should operate in real-time with short window times (<0.5 s) and minimum gap between windows. Provision to achieve by software a characteristic equivalent to a time constant of 1.5 s should be provided.

The standard states that in cases of doubt where the limits are exceeded, a reference monitor is to be used. This is an analog type with a 3 Hz (±0.5) bandwidth between points at -3 dB and a minimum attenuation of 40 dB for a single injected frequency signal at a frequency equal to $f_n - 15$ Hz or $f_n + 15$ Hz for harmonic order n.

2.3 A Review of Harmonic Monitors

Harmonic monitors are instruments designed to find harmonic components of power system current and/or voltage signals. In addition to these quantities, they can often also compute harmonic phase, power and impedance, and such parameters as THD, EDV, and EDI. They are usually equipped with a display, a printer for hard copies, and occasionally a disk drive for storing harmonic data. Harmonic monitors ideally track variations in the fundamental frequency so that the harmonic outputs represent the true harmonics of the fundamental. This is distinct from more general signal analyzers (which include spectrum analyzers and Fourier analyzers), such as the HP3561A dynamic signal analyzer [Hewlett Packard, 1992], which offers a very high frequency resolution (resolving inter-harmonic signals), but cannot track rapid changes in the fundamental frequency. Signal analyzers are not aimed specifically at power systems, and therefore quantities such as EDI, EDV, and units for current must be calculated by hand.

Harmonic monitors can be divided into two main categories. The first category is that of analog instruments, which usually employ a single adjustable notch filter for tuning to a particular harmonic [Arrillaga, 1982]. The notch filter uses either a heterodyne system or a direct tunable selective filter to observe one particular harmonic. For real-time analysis of all harmonics, a parallel array of notch filters is required, although the implementation of this is not very practical. Analysis time can be reduced by recording a signal and playing it back many times faster. This can also be used for multichannel analysis by using a multi-track tape recorder. The only form of display for analog instruments is a meter, and recordings of harmonic levels must be made by hand or by a pen recorder. An example of an analog harmonic analyzer is the *Selective Audio Frequency Power Spectrum Analyzer* (SAFPSA) described in [Edward *et al.*, 1981].

The second class of instruments, digital instruments, are the result of the application of computer technology to monitoring harmonic levels. In digital instruments voltage and current signals are sampled and quantized to discrete levels which are converted to digital samples for machine computation. The FFT is invariably used to convert the sampled signals to harmonics. Presentation of harmonic levels is achieved by either displaying voltage or current versus harmonic order on a screen or producing a print out of the levels of each harmonic. The following section reviews some of the most prominent digital harmonic monitoring equipment either available commercially, or developed through University research.

2.3.1 Digital Instruments

Due to the processing demands of continuous real-time harmonic monitoring, most digital harmonic monitors work on a 'snapshot' basis, where a number of periods of the waveform under investigation are acquired, stored, and then processed in non real-time. The processing is usually achieved by a general purpose processor that is also responsible for the operation of the instrument as a whole. Some of these instruments are Personal Computer (PC) based, using a data acquisition card to acquire voltage and current signals, the PCs micro-processor to compute harmonic levels, its hard disk to store data, and the PC display to display harmonic levels. Other monitors are dedicated instruments, with built-in display units and printers. The following sections give a

brief description of each monitor with their relevant features. Sections 2.3.1.1 to 2.3.1.4 review commercially available monitors, while Sections 2.3.1.5 to 2.3.1.9 review monitors developed as research projects.

2.3.1.1 The BMI 3030A Power Profiler

The Basic Measuring Instruments (BMI) 3030A power profiler is intended as a general purpose three phase power analyzer for harmonic analysis, energy management, and demand management. Its features regarding harmonic monitoring are [BMI, 1992]:

- Three phase harmonic voltage and current computation and display.
- Built in printer for hardcopies of results.
- Clamp-on current probes.
- Sequence information of harmonics.
- Harmonic power snapshot for direction of harmonic flow.
- Total harmonic distortion information for voltage and current is available in meter readings, summaries and snapshots.
- Display of up to 4 individual harmonics against time on any one graph.
- The generation of snapshots of 4 selected harmonics when any of the 4 exceed a pre-selected limit.
- Snapshot list of voltage or current harmonics up to the 50th (magnitude and phase).
- Snapshot graph of the harmonic spectrum up to the 50th harmonic.
- Transformer derating calculation.
- Telephone interference factor calculation.
- Harmonic voltage is displayed as a percentage of the fundamental.
- Harmonic current can be displayed as a percentage of the fundamental or as a percentage of maximum load.

This instrument uses a phased-locked sampling technique to follow variations in the mains frequency. It is a snapshot system, and is limited to 3 voltage channels and 3 current channels. Details regarding its exact harmonic analysis technique (the FFT record length and whether it uses averaging) are not available. Data are presented as hardcopies on paper from a small built-in printer. Reports of harmonic data can be generated from this at regular intervals. A 720 kb floppy disk drive is optional. Data from this can be transferred to a PC and analyzed using BMI software. Inputs to this instrument are analog signals, requiring isolation from their high voltage sources if the instrument is to be protected.

2.3.1.2 The Dranetz Series 901 Power Harmonic Analyzer

This is a single-phase analyzer designed to measure the following parameters of any single-phase branch circuit [Dranetz Technologies, 1989]:

- Harmonic voltage (actual volts for the fundamental and percentage of the fundamental for harmonics) up to the 25th harmonic.
- Harmonic current (actual amperes for the fundamental and percentage of the fundamental for harmonics) up to the 25th harmonic.
- Fundamental power (watts).
- Harmonic power (watts).
- Power factor.
- Total harmonic voltage distortion.
- Total harmonic current distortion.

All of this information is automatically printed out at pre-selected intervals by a built-in printer. Inputs to this instrument are analog, requiring isolation from their high voltage sources if the instrument is to be protected. No information relating to the method of harmonic analysis used is available.

2.3.1.3 HP 3565S Measurement Hardware

The HP 3565S measurement hardware is a typical example of the use of data acquisition equipment for harmonic analysis. It was used by Transpower New Zealand Ltd. during the commissioning of the upgraded Inter Island HVdc link (discussed in Chapter 7) for a variety of purposes. Its main use was in transient analysis, although it was used to acquire data for harmonic analysis. The harmonics of the acquired data were computed using the mathematical analysis package MATLAB, which gave a high degree of flexibility in computing harmonics, but was slow, and worked on a snapshot basis.

The HP 3565S measurement system consists of a host computer to which seven different types of modules may be attached. These are listed below together with a brief description.

- Signal processing module: Used to control data flow between modules, host computer, and disk. This can execute downloaded programs from application software. It uses a Motorola 56001 DSP with 1 Mbyte of Random Access Memory (RAM), processing data acquired by the input modules.
- Analog input module: This is a 13 bit dual channel analog to digital convertor module for acquiring data for measurements from dc to 51.2 kHz. A separate 13 bit analog input module is available for acquiring data for measurements from dc to 102.4 kHz.

- 8-channel input module: This is a 12 bit 8 channel analog to digital convertor module for acquiring data for measurements from dc to 12.8 kHz. All channels are sampled simultaneously, and a maximum of 32 of these units can be added to a system.
- Source Module: This is used as an analog output module, as well as a signal source for calibrating the input modules.
- Programmable DAC : A Digital-to-Analog Convertor that can be programmed to produce a user defined signal.
- Parallel Interface Module: This handles the interface between all modules and the host computer.

The HP 3565S system has the capability of acquiring many signals via its 8 channel input modules under software control. This avoids the need to physically swap signals round at the inputs. This makes it a very powerful data acquisition system, which has a certain amount of processing capability offered by its signal processing module. However this is not capable of processing the data from all channels simultaneously. Consequently for harmonic analysis of many channels, it can only be used as a snapshot system.

2.3.1.4 The NOWA 1 Harmonic Monitor

The NOWA 1 is a two channel voltage and current harmonic monitor designed primarily for the low voltage network (100 V to 400 V), meeting the requirements of the EN 50 006 or IEC 555 (edition 1982) standards for domestic loads.

The NOWA 1 works on a snap shot basis, acquiring 320 ms snap shots of the voltage and current input signals once per second and computing the harmonics of these using an FFT. Sampling is synchronized to the fundamental component, and the out of band attenuation is greater than 60 dB for signals which are separated from the centre frequency by more than 22 Hz. The 1.5 s time constant on the output required by the EN 50 006 / IEC 555 standards is achieved using staircase averaging on the computed harmonics.

The NOWA can also compute RMS values of voltage and current, true reactive and apparent power, power factor, and the fundamental frequency of the input signal. Its output is in the form of a display that can show harmonic voltage or current versus harmonic order, and a strip printer that produces a list of harmonic voltages (percentage of the fundamental) or currents (amperes) versus harmonic order.

2.3.1.5 Hungarian Research Institute Research

The Hungarian Research Institute for the Electrical Industry have developed a multi-purpose instrument that can be used both as a multimeter and an analyzer, and is reported in [Papay *et al.*, 1990]. It is a two channel instrument designed to measure the characteristics of sinusoidal or non-sinusoidal voltage and/or current, giving such quantities as the fundamental and harmonic voltages, currents, active and reactive power, phase angles, and power factor. It measures up to

the 13th harmonic, using a Z-80 micro-processor assisted by a floating point arithmetic processor for harmonic computation. A graphic processor is used for data display on the instruments built in CRT display. A floppy disk drive can be attached to the system for storing measured data, and the instrument can be operated by remote terminals via an RS-232 link (using an IBM PC for instance). The instrument is a snapshot system - it cannot compute the harmonics of each cycle and subsequently analyze these in real-time, archiving only the relevant data.

2.3.1.6 Georgia Institute of Technology Research

The School of Electrical Engineering at the Georgia Institute of Technology carried out a feasibility study investigating the requirements for developing and implementing an on-line harmonic measuring system for the New York State Extra-High-Voltage (EHV) grid in conjunction with the New York Power Authority. The results of this study are reported in [Zelingher *et al.*, 1990] and in [Meliopoulos *et al.*, 1992].

In their study they conclude that existing voltage and current transformers will influence the accuracy of measurements, and identify the need to characterize them and correct computed harmonic components. They also require a system that will make synchronized measurements of voltage and current at selected substations.

The system is PC based and uses a PC data acquisition card to acquire voltage and current signals. Multiple PC based units are located at various sites on the EHV network, and are connected to a master workstation via telephone lines. The PCs acquire a 0.5 s snapshot of data from each transducer at predetermined time intervals (either every 10 or 15 minutes), compute the harmonics of the data (up to the 25th harmonic), correcting for errors caused by transducer frequency response irregularities, store the data on their local hard disk, and send harmonic results to the master workstation. Acquired data is time tagged to enable comparison with data acquired from other sites using the substations reference clock. The system is only capable of performing harmonic analysis on a snap shot of data, although it can do this repeatedly, and is designed to run unattended for long periods.

The use of harmonic state estimation software that uses the harmonic measurement data collected by the master workstation from nominally 12 monitoring sites is described in [Meliopoulos *et al.*, 1992]. This estimates harmonic voltages and currents at all nodes of the power transmission system based on the data collected from the 12 monitoring sites.

2.3.1.7 Research at the Queensland Institute of Technology, Australia

A three voltage channel and five current channel harmonic analyzer developed in the School of Electrical and Electronic Systems Engineering at the Queensland Institute of Technology is reported in [Littler, 1988]. This is a snap shot system based on the Motorola 6802 microprocessor. It samples synchronously with the fundamental frequency, and measures up to the 21st harmonic. Output is in the form of a printout which gives the fundamental frequency, voltage or current harmonic magnitudes (RMS volts or amperes), and voltage or current phase.

2.3.1.8 Worcester Polytechnic Institute Research

This section summarizes the research carried out at the Worcester Polytechnic Institute into the design of a system for automated measurement and statistics calculation of voltage and current harmonics. Their work is reported in [Orr *et al.*, 1986], which was presented at the IEEE power Engineering Society 1986 Winter Meeting.

The system is 8086 PC based, using a seven input analog to digital conversion card, allowing 3 voltages and 4 currents (including the neutral current) to be monitored. Sampling is synchronous with the fundamental frequency.

The instrument can store and display the mean, mean square value, variance, maximum, and minimum for each harmonic of each channel over a period of N hours, divided into subintervals of length T seconds. The telephone influence factor and total harmonic distortion may also be calculated over the entire interval, and probability distributions of magnitude and/or phase angle can be calculated as histograms.

The measurement is almost completely software controlled, with a menu-driven setup for establishing the measurement conditions - such as transducer type for each channel (voltage or current transducer) and transducer ratio, input gain, current shunt value, total measurement time, and measurement interval.

The harmonic measurement system is clearly not real-time, only taking snapshot measurements every T seconds with the processing performed by the PC's 8086 micro-processor. The inputs to the monitor are analog, which require isolation from the high voltage system under test if the instrument is to be protected.

2.3.1.9 The MAC-8 System

The MAC-8 data acquisition system for automatic harmonic measurements was developed between 1975 and 1982 by the then New Zealand Electricity [NZE, 1973]. Its primary purpose was to monitor and record harmonic levels at points on the NZE transmission system for line voltages of 66kV and above, and to assess compliance with the "Limitation of Harmonic Levels Notice" [NZED, 1983].

It was originally intended as a controller and data acquisition unit for the SAFPSA spectrum analyzer [Edward *et al.*, 1981] to provide an automatic harmonics monitoring system. However the SAFPSA was abandoned in favour of the FFT due to problems experienced in adapting it to automatic measurement. Two MAC-8 systems were produced, each housed in a caravan for towing to any measurement site in New Zealand.

The MAC-8 is based on a specially built minicomputer for the fast data acquisition and processing required by harmonic measurement. It can find up to the 50th harmonic of three voltage and three current channels, and uses a synchronized sampling technique. Computed harmonic levels are compared with a threshold of the limits set out in [NZED, 1983], and are stored on tape if any thresholds are exceeded. The system can monitor any point of common coupling for over one week, with stored data analyzed after monitoring. It is a snapshot system, with data acquired from each channel once per minute. Data stored during monitoring is analyzed

after monitoring by a large mainframe computer, which usually takes several weeks to complete.

2.4 Conclusion

Because of the detrimental effects of excessive harmonic levels on a power system, many countries have introduced standards limiting harmonic voltages at points of common coupling and harmonic currents produced by distorting loads. The standards deal with various types of loads by grouping them according to size, leading to standards that deal with domestic loads and industrial loads separately. Standards for industrial loads also deal with the transmission system and distribution system separately.

As well as specifying limits, standards also set out requirements for harmonic monitoring instrumentation. A review of the salient harmonic standards illustrates that the main requirement of harmonic monitoring equipment is to find harmonic voltage and current magnitude levels. Additionally they accept the use of DFT analyzers, giving permissible errors in measuring voltage and current harmonics. However, different standards vary according to how harmonic levels are to be computed using the DFT, generally specifying different window lengths, or requiring averaging of the data prior to the DFT. They also have different requirements for processing of data after the DFT, with some requiring averaging, and others giving no specific details.

To meet the diverse requirements of the different standards clearly requires a very flexible instrument - one of the main factors influencing the design of the CHART instrument, which has inherent flexibility because processing is performed in software. This approach allows different processing techniques, tailored to meet the requirements of particular standards or even research requirements, to be applied in different situations by loading the appropriate software onto a common hardware 'platform'.

The CHART instrument has been designed to have the selectivity and time constant required by New Zealand legislation. By using precision components in the data acquisition stage, high accuracy analog to digital convertors, and 16 bit digital arithmetic the error in computing voltage and current harmonics is minimized. Nevertheless, it is difficult to put an absolute accuracy on these measurements, as the instrument relies on its connection to the power system to obtain accurate information on the harmonic content of currents and voltages. Suffice it to say that CHART has been designed to be very precise to 'decouple' it from the inaccuracies of voltage and current transformers.

Other harmonic monitors that perform processing in software have been developed, although these tend to process many channels of data in a single processor. This ultimately restricts the number of channels that can be investigated due to the processing speed of the single processor, and due to bus bandwidth limitations encountered in actually getting data from their sources to the processor. By distributing processing amongst data acquisition channels, the CHART instrument avoids these problems by actually processing and reducing data at its source. The following chapter covers the design of the first prototype of the CHART instrument, discussing its connection to a power system, its processing system, and its data display system.

Chapter 3

THE CHART I HARMONIC MONITOR

3.1 Introduction

The CHART I harmonic monitor began as the Harmonic Analysis and Instrumentation Project (HAIP) in 1986 with financial support from the then New Zealand Electricity Division. At that time a decision to use a new bus standard for the instrument, known as Multibus II, was made. Multibus II is an Intel multi-processor system bus standard, and at the time was considered technically superior to other available bus architectures such as VME. It was also anticipated that processor technology for Multibus II would soon match the requirements for multi-channel real-time harmonic monitoring. Because of the requirement for real-time harmonic analysis up to the 50th harmonic for multiple channels, as well as the need to compact, store and display harmonics, the instrument was designed by partitioning it into functional units. Each unit consists of a microprocessor subsystem, and uses the Multibus II Parallel System Bus (PSB) to communicate with other units. The features of Multibus II and the way they are used in the CHART instrument are discussed in Appendix 5A. Unfortunately Multibus II did not gain wide market acceptance as quickly as anticipated compared to its main rival, VME. Consequently the processor cards that were desirable for harmonic analysis did not emerge, and the monitor had to be built around the Multibus II processor cards that were available at the time. Progress on the monitor was also hindered by delays in introducing the bus interface device (the Message Passing Co-processor or MPC) and in the development of the iRMX operating system to a level that would fully utilize the bus capabilities.

This chapter introduces the environment in which the harmonic monitor must operate and covers the data acquisition system and Multibus II subsystems that make up the monitor, from the acquisition computer to the FFT computation subsystem, through to the compaction and storage subsystem. Harmonic data display in the instrument is achieved by use of a custom designed windows environment operating on a PC, which is also discussed. The chapter is concluded by a discussion on the achievements made with CHART I.

Much of the ground work with the Multibus II software was performed by Norman Hadfield as part of a Masters degree [Hadfield, 1988], while the windowing software for the PC was written by Alex Bould, also as part of a Masters degree [Bould, 1988].

3.2 The Monitoring Environment

The monitor relies on its connection to the power system to obtain accurate information of the currents and voltages and yet needs to be adequately isolated from the electrostatic and electromagnetic effects of the high voltage system.

The inputs to the monitor comprise six analog voltages transmitted from transducers by fibre optical cables. These signals are obtained from current and voltage transducers located at appropriate points of the network.

To reduce the signals' dynamic range to a level suitable for transmission through fibre optical cables, the fundamental component is attenuated by passing each signal through a highpass filter, with a cut-off frequency at the 2nd harmonic. This leaves the harmonics unattenuated, maintaining them above the noise level. The magnitude and phase change in the signals, introduced by the transducers, interfacing circuitry, and signal conditioning equipment are required to be compensated for in the frequency domain after their DFTs have been computed.

The fibre optic cables provide an effective means of isolating the signal processing equipment within the monitor from the high voltage power system equipment. The original specification for the interface of the monitoring instrumentation and the transducers was made by the New Zealand Electricity Division [Goodwin, 1986]. The interface and related signal conditioning are illustrated in the schematic diagram of Figure 3.1

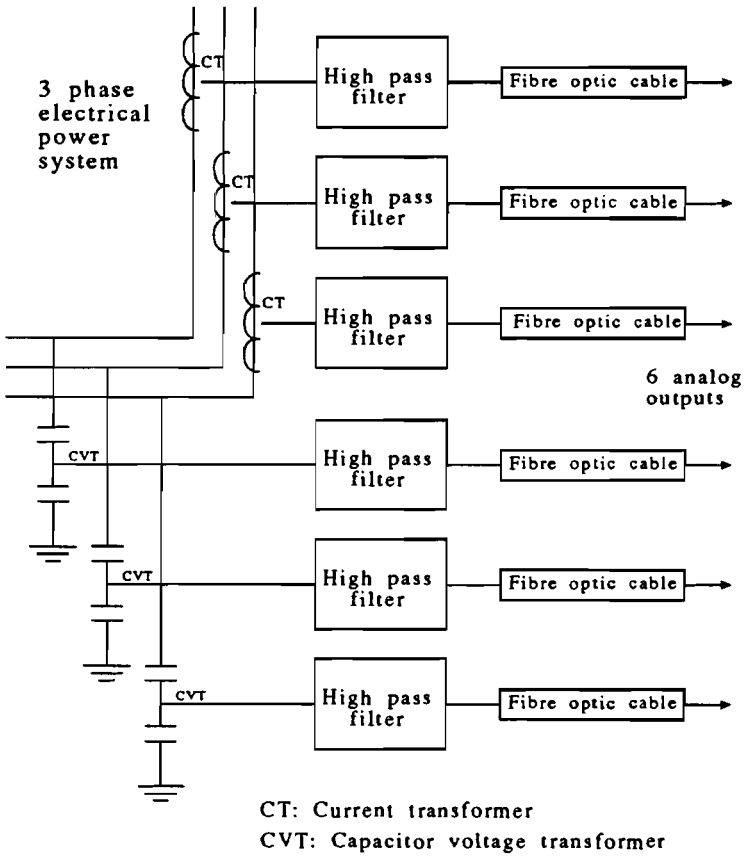


Figure 3.1 Electricorp interface and signal conditioning equipment.

3.3 The Structure of the Harmonic Monitor

This section describes the hardware, software, and operation of the CHART I harmonic monitor. The monitoring system consists of three main components: (i) a dedicated signal conditioning and data acquisition system, (ii) a Multibus II multiple processor system, and (iii) an IBM compatible PC-AT. These are illustrated, together with their interconnections, in Figure 3.2.

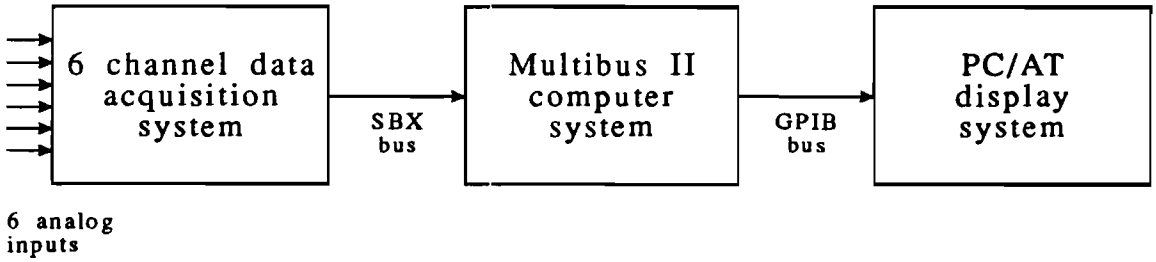


Figure 3.2 The CHART I Harmonic Monitor Structure.

The dedicated data acquisition system is designed specifically for the purpose of acquiring six analog voltages simultaneously from external power system transducers and converting them to digital samples suitable for computer processing. Time domain data are converted to harmonic data in the Multibus II system, which are stored for later retrieval and analysis. Harmonic data are retrieved and displayed on an IBM compatible PC-AT which is connected to a Multibus II computer by a General Purpose Interface Bus (GPIB).

3.3.1 The Data Acquisition System

Figure 3.3(a) illustrates one channel of the data acquisition system. Each of the inputs fed to the data acquisition system is passed through an anti-aliasing filter. This filter attenuates frequencies above the 50th harmonic to reduce errors caused by aliasing. The signals on each channel are sampled and held simultaneously in order to provide time synchronous signals for subsequent sequential analog to digital conversion, which achieves accurate 12-bit digital representations of the analog signals.

The sampling signal is produced by the *Sample Rate Multiplier* (SRM) which has the primary purpose of adjusting the sampling interval in order to maintain it at an 'exact' $\frac{1}{128}$ sub-multiple of the fundamental period (it effectively accommodates the small changes that may occur in the mains frequency). This device combines an 8751 Intel micro-controller, and a high speed counter (operating at 22 MHz), to produce 128 sampling pulses, uniformly spaced in time, within one period of the fundamental waveform. Hence a rectangular window is effectively applied over one period of the fundamental, virtually eliminating the problem of spectral leakage [Brigham, 1974]. The signal conditioning performed to provide the zero crossings of the fundamental wave is illustrated in Figure 3.3(b). The SRM is discussed in Section 5.2.2.3.

The output of the Analog to Digital Convertor (ADC) is a parallel signal which is stored in a First-In-First-Out (FIFO) buffer. This provides some buffering between the data acquisition system and the Multibus II data acquisition computer. The data acquisition system also makes an

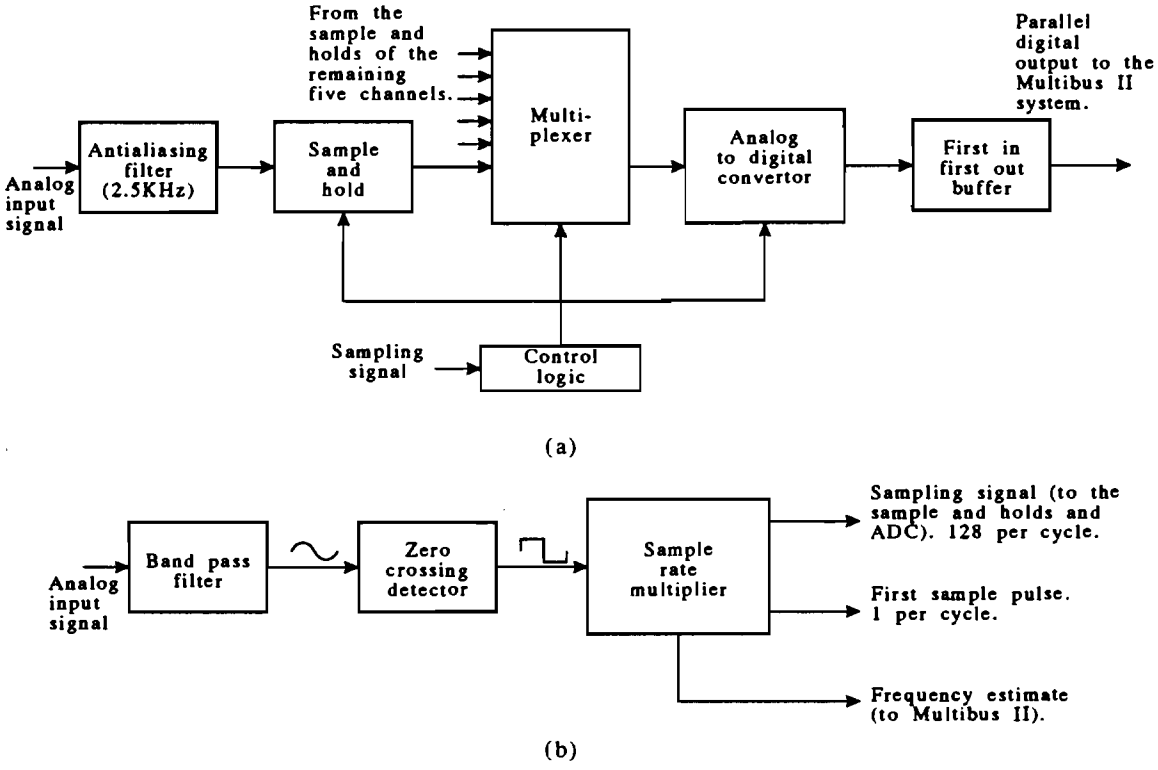


Figure 3.3 (a) One channel of the data acquisition system. (b) Production of the sampling signal.

estimate of the fundamental frequency at the time of measurement. This information is transmitted with the digitized signals to the Multibus II data acquisition computer.

3.3.2 The Multibus II System Computers

The data 'captured' in the previous stage still requires considerable transformation to be in a useful form for analysis. It is averaged to reduce computation requirements and the effect of non-harmonic signals present in the acquired signals (discussed in Section 6.4), transformed from the time domain to the frequency domain using an FFT algorithm and then processed to store not only the raw harmonic data, but also derived information such as maxima and average levels encountered. Finally the stored data must be made available for further purposes, such as display on the PC-AT, or control purposes designed to reduce the detected harmonics levels.

A system which provides a multi-processor environment, such as Multibus II, enables the separation of the processing requirements into three main parts, with each part performed by a separate Single Board Computer (SBC), as illustrated in figure 3.4. The detailed implementation of software on each computer is discussed in full in [Miller *et al.*, 1990].

3.3.2.1 The Acquisition Computer

Information from the data acquisition system passes directly to the memory of the acquisition computer. This is a Micro Industries Multibus II prototyping computer based on the Intel 80186 micro-computer [Micro Industries, 1987], and is referred to as the 186/110A board. It incorporates

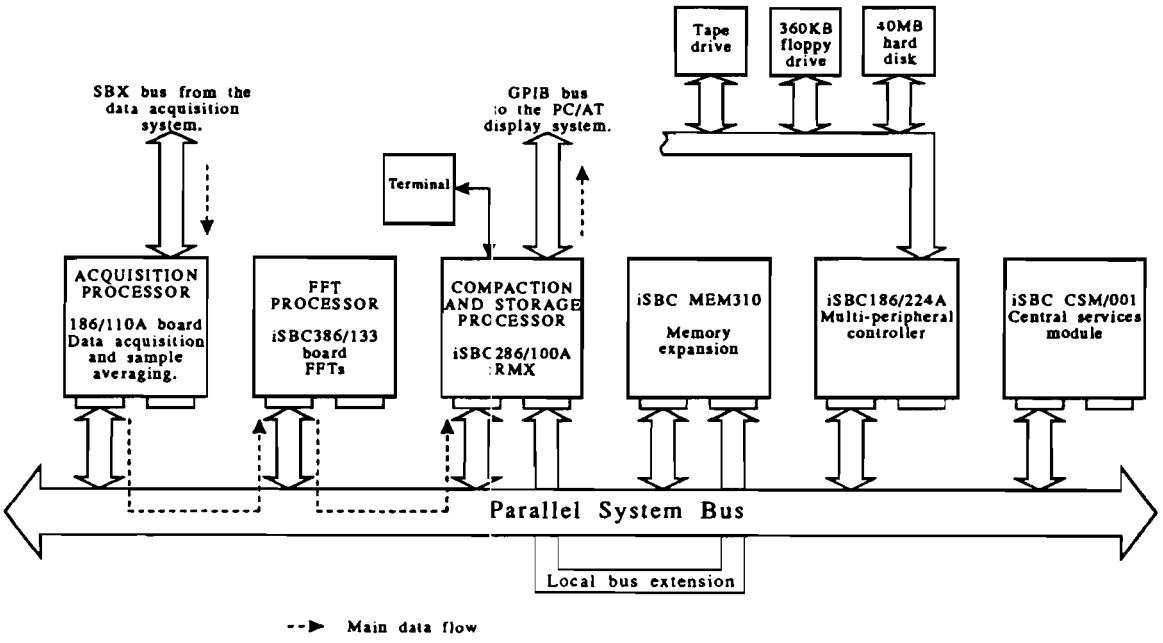


Figure 3.4 The Multibus II system configuration, showing the functions performed by each computer in the system.

a complete interface to Multibus II using the MPC, the 80186, and the 8031 micro-controller used to implement interconnect space. It also has a Direct Memory Access (DMA) unit, 512 kb of Dynamic RAM (DRAM), 128 kb of Erasable Programmable Read Only Memory (EPROM), an RS232 serial port for terminal communications, an Intel iSBX bus, and a free area for prototyping designs. With these features it acts as a platform to prototype designs for Multibus II boards without the need to design and produce the complete bus interface. In this design the iSBX bus on this board is used to interface the data acquisition system with Multibus II, as it provides adequate bandwidth for 6 channels sampled at 6.4 kHz each. The 186/110A board runs a simple operating system written by the author which provides critical functions such as board initialization, Multibus II message passing and interconnect space support, terminal communication calls, data acquisition drivers, and a boot-loader. This operating system and the development of the boot-loader is described in full in [Miller *et al.*, 1990]. Multibus II message passing concepts and interconnect space concepts are covered in Appendix 5A.

In addition to acquiring data, the acquisition processor averages each of the six channels of time domain data over five cycles of the fundamental component, producing one averaged cycle per channel. This reduces interference from non-harmonic frequencies present in the signal (discussed in Section 6.4), as well as reducing the rate of data being FFT transformed, thereby reducing the requirements of the FFT computer.

The averaged data are formed into packets, which are queued by the acquisition computer, ready for passing to the FFT computer via the Multibus II message passing system. The bulk of data movement onto and off the acquisition computer is handled by DMA devices, and interrupts are used to handle incoming data and Multibus II messages (which are in fact bus interrupts). The code is written in the Intel PL/M high level language with MOD186 to support the 80186 micro-

computer, and with a small amount of Intel ASM86 assembler used in initialization stages and in time critical sections of the code (the averaging algorithm for instance). The source code is written in separately compiled modules with their own initialization structures allowing each task to be managed effectively. The software for this computer was developed on the Intel iSBC286/100A single board computer running the iRMX286 Release II.4 operating system and loaded into the 180/110A target system using the boot-loader discussed in [Miller *et al.*, 1990].

3.3.2.2 The FFT Processor

The FFT processor is a standard Intel Multibus II 80386 based computer that runs at 20 MHz. It uses a radix-2 FFT algorithm to compute the DFT of the averaged time domain data received from the acquisition processor. The requirement that the data be transformed in real-time ultimately restricts the number of channels that can be handled by this board. It was originally intended to use a Multibus II array processor card to implement the FFT, however this was unavailable at the time. The transformed data packets are queued ready for message passing to the compaction and storage processor.

This 386 computer is running in its 8086 mode which maximizes its processing capabilities. It also runs an Intel supplied Built In Self Test (BIST) prior to loading its application from the master Central Processor Unit (CPU) using the boot-loader discussed in [Miller *et al.*, 1990]. The application initializes the board and then creates queues for averaged data to arrive from the data acquisition board and queues for FFT data to go to the main CPU board. Interrupt service routines and DMA transfer routines service the reception and transfer of data from the acquisition board and to the main CPU.

The software is written in PL/M86 and ASM86 as a set of modules. The data arrives from the data acquisition board at intervals of five cycles of the fundamental frequency (100ms for 50Hz). The software receives a message of time-domain-averaged sample packets, applies the FFT algorithm to each of the packets, and then sends the data to the next board.

To achieve this task the FFT algorithm has been written in PL/M86 and then hand optimized in assembler [Hadfield, 1988]. The resulting algorithm including all message passing takes typically 80 percent of the processing power of this board. All arithmetic is performed using 16 bit fixed point number representation, with scaling after each stage of the FFT to avoid overflow [Hadfield, 1988].

3.3.2.3 The Compaction and Storage Processor

To enable the inspection of harmonic levels at a later time, or at a location other than in the field, the harmonic data are compacted and stored on a hard disk.

The compaction and storage process takes data from the FFT processor and compacts it by averaging over one second intervals. A time stamp from the corresponding time domain source data is appended to every FFT packet, enabling the precise identification of the time of measurement of the raw data.

The compaction and storage computer is based on the 80286 processor and is the master CPU in the Multibus II chassis, running the iRMX286 II.4 operating system. This computer downloads

the applications to the acquisition and FFT processors as described in [Miller *et al.*, 1990]. After login the user is able to start either or both of two main applications - 'compaction and storage' and 'retrieval and replay' documented below.

Access to the disk drives is gained using a Multibus II peripheral controller computer (shown in figure 3.4) which is configured into the RMX operating system running on the compaction and storage processor. Standard RMX operating system calls to disk drives are therefore supported via this computer.

3.3.2.4 The Retrieval and Replay Task

The set of 'readings', stored on disk, may be required for display and/or further analysis. The retrieval task reads the selected data items back into memory from hard disk and sends them via the GPIB bus to the PC.

The multitasking capability of RMX286 is used to enable the retrieval task to operate concurrently with the compaction and storage task on the same CPU, but at a lower priority. The two tasks are started from completely separate logins, which allows the instrument to be recording one set of 'readings' while displaying a completely separate set of 'readings' from another occasion. The monitor will also display in real-time the same set of 'readings' that are being recorded.

The algorithms for compaction, storage and replay are written in PL/M286 and rely heavily on the iRMX286 multitasking operating system for aspects of priority, message passing over Multibus II and file storage and retrieval. The code for interfacing to the GPIB bus (which plugs into the iSBX bus of the compaction computer) was written and tested locally. Each section of code is written as a separate module, which aids the maintenance of complex programs.

3.3.3 The PC/AT Display

The user interface to the CHART instrument was considered an important feature of it, as the ease with which the system may be configured to perform desired operations ultimately determines its popularity, and is conducive to its correct use.

The user interface to this instrument is a custom written mouse driven windowing system and uses icons (graphically drawn keys) to provide a very comprehensible instrument interface.

Data are displayed as graphs of harmonic voltage, current, impedance, and power against harmonic order. Both the magnitude and phase of these variables can be displayed. Each graph is contained in a separate window, and the windowing system enables a user to lay out the display to suit particular requirements. This is achieved by enabling a user to move a window about on the display, shrink or enlarge it, and/or to completely remove it.

It addition to the graphs, the actual fundamental frequency is shown on the display, and an indication of whether or not it is within the prescribed limits is also shown.

The PC/AT software is written exclusively in MODULA-2. MODULA-2 has *multitasking* built into the language which permits the writing of a *schedular* for concurrently executing tasks or processes. The schedular uses message passing as its only method of synchronization. The use of the schedular permits further decomposition of the PC/AT software into tasks even though

PC-DOS (PC Disk Operating System) itself does not allow multi-tasking. The schedular takes care not to allow the interruption of tasks that are using PC-DOS operating system calls; this may cause corruption of the operating system as many PC-DOS calls are not re-entrant.

The long term plan for the user interface and graphical harmonic display was to incorporate it into Multibus II when a suitable graphics card became available.

3.4 Conclusion

This chapter has described an harmonic monitor for which software has been developed to provide the type of information required by current New Zealand legislation [NZED, 1983], although many future requirements can be accommodated without altering the hardware structure. A prototype of the monitor was completed in May 1990 and was initially operated in a controlled laboratory environment where it was calibrated and prepared for use in the field. In July 1990 it was taken to the Islington substation in Christchurch, New Zealand, and used to monitor harmonic levels. This exercise is discussed in the next chapter.

The work with this monitor lead to the publication of a paper in the proceedings of the 1990 4th International Conference on Harmonics in Power Systems (ICHPS4) in Budapest, Hungary [Lake *et al.*, 1990], and in the proceedings of the 7th International Conference of the Intel Real-Time Users Group (iRUG) in St. Louis, Missouri, USA [Miller *et al.*, 1990].

Chapter 4

HARMONIC MEASUREMENTS USING CHART I

4.1 Introduction

This chapter documents field tests performed with the CHART I instrument introduced in the previous chapter during July 1990 at the Islington Substation in Christchurch [Miller and Dewe, 1992a], [Miller, 1990]. It discusses the connection of the instrument to the system and identifies a number of practical issues associated with such an exercise. In particular, issues associated with interfacing such equipment to the power system voltage and current transducers via fibre optic links are addressed, together with details of the necessary on-line compensation for the characteristics of the transducers, fibre-optic links and associated signal conditioning circuitry. The limitations of the CHART I monitoring system are identified and improvements to the system leading to CHART II are discussed.

4.2 Harmonic Measurements

With the co-operation of the Electricity Corporation of New Zealand, the prototype CHART I system was used to monitor harmonic levels at the Islington end of the Islington - Twizel 220kV transmission line illustrated in Figure 4.1(a). Design Power New Zealand's fibre optic harmonic monitoring system was used to isolate the instrumentation from voltage and current transformer connections in the Islington switchyard, as discussed in Section 3.2. Figure 4.1(b) shows the location of the Current Transformers (CTs) and the Voltage Transformers (VTs) used for the tests on the transmission line. Conventional protection CTs and Capacitor VTs (CVTs) were used to provide replicas of the line current and bus voltage waveforms. These have unknown low pass frequency responses which will have affected the results obtained - especially the voltage harmonics [Meynaud, 1989], [Arrillaga *et al.*, 1985a]. However there was no alternative, and as the purpose of the exercise was to evaluate the system rather than the end results, these were considered adequate. Due to data storage limitations of the system as it was configured then, harmonic levels were only monitored and stored for up to one hour. This was performed several times throughout the tests, storing the results on streaming tapes at the end of each session.

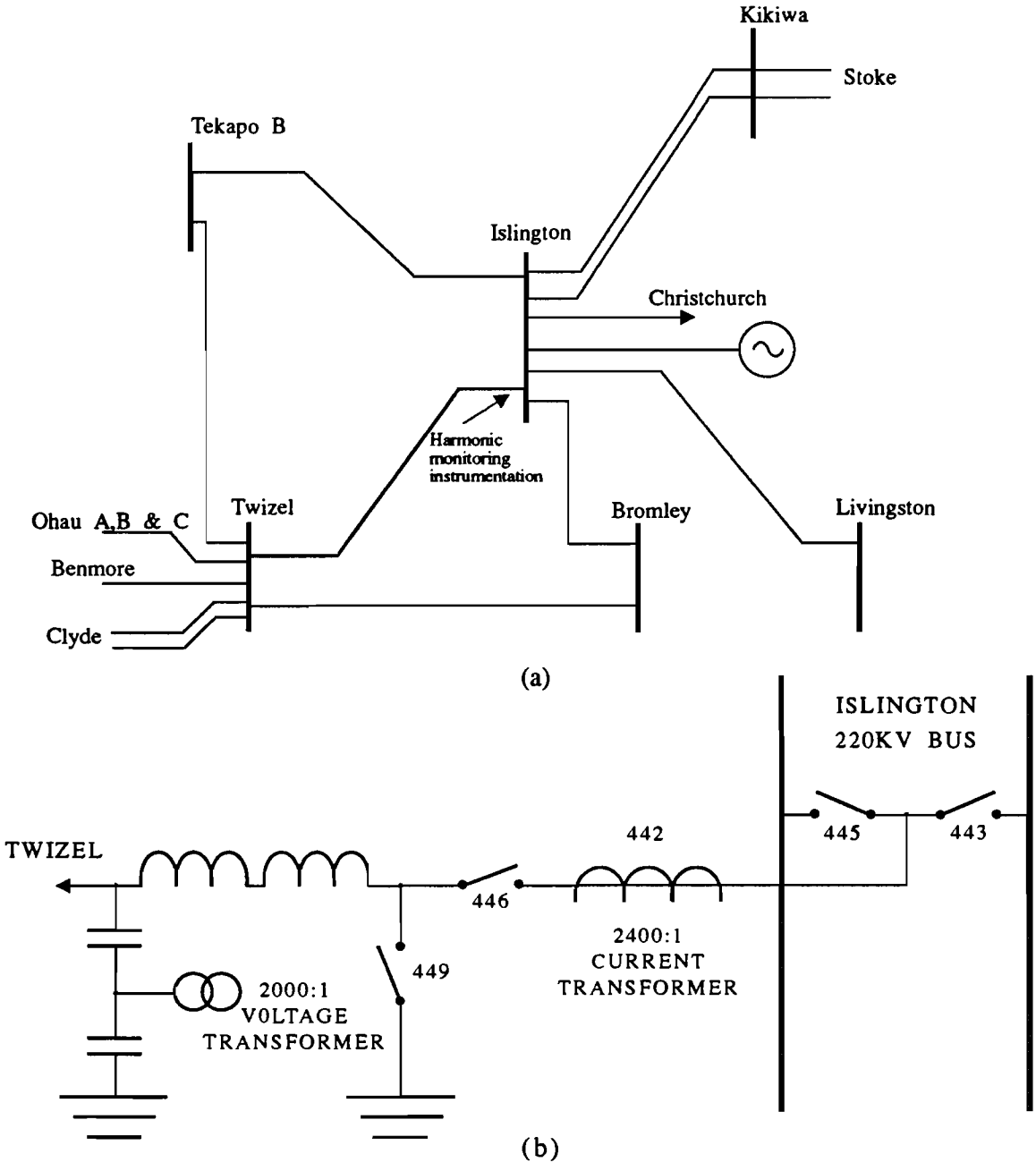


Figure 4.1 (a) The harmonic monitoring instrumentation connection to the New Zealand South Island 220kV power system. (b) Current and voltage transformer locations used for testing.

4.2.1 Design Power New Zealands Fibre Optic Harmonic Monitoring System

The Design Power harmonic measuring fibre optic system illustrated in Figure 4.2 is an analog FM system specifically intended for analysis of signals on in-service high voltage equipment. This transmission system has a dynamic range which, in the presence of the fundamental component, is too low for the reliable determination of voltage and current harmonic levels, which are generally below the noise floor of the transmission channel. This problem is circumvented by preceding the transmission system with high pass filters designed to attenuate the fundamental frequency,

thereby allowing the amplification of harmonic levels above the noise floor [NZE, 1973]. High pass filtering is a recognized technique for use in systems with a limited dynamic range [Pesonem, 1981], although it requires compensation for the filter responses - another computational burden and source of error. Compensation for the filters (as well as the optical transmission system and data acquisition system anti-aliasing filters) was achieved by multiplying harmonic magnitudes by lookup tables, determined from the filters in the laboratory. The phase response of the filters was compensated for by adding the inverse filter phase responses to the harmonic phase results - also determined in the laboratory [Miller, 1990]. The high pass filter magnitude responses are shown in Figure 4.3. Unfortunately these high pass filters attenuate the fundamental component so severely that it is extremely difficult to reliably amplify it back to its original level given that the fundamental frequency of a power system varies continuously [Miller, 1990]. Nevertheless, this system is adequate for assessment of compliance with New Zealand legislation which does not require the fundamental component [NZED, 1983]. However, for more thorough research (such as harmonic impedance determination and harmonic power flow) the fundamental component is important [de Oliveira *et al.*, 1989]. One channel of the six channel (three phase) fibre optic transmission system was not functional during the tests, preventing the CHART I system from computing the yellow phase current harmonics.

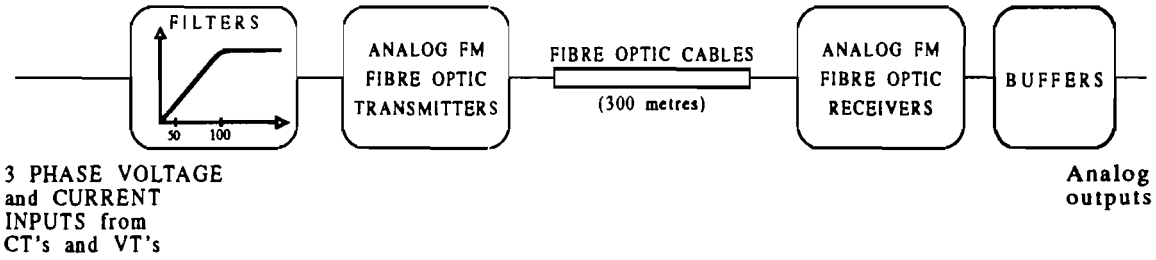


Figure 4.2 Design Power New Zealands Fibre Optic Harmonic Monitoring System.

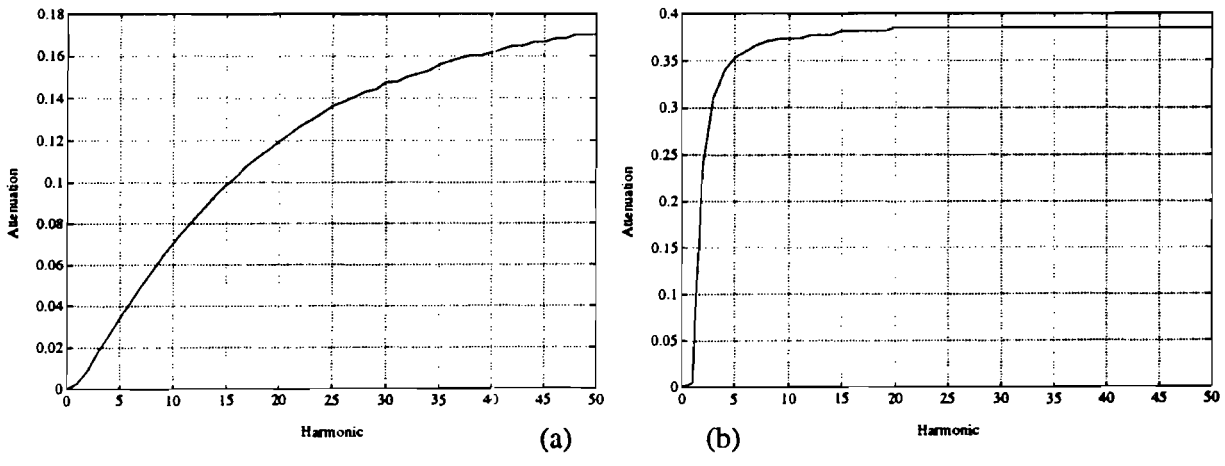


Figure 4.3 Fundamental suppression filter responses (identical for all phases) for (a) the voltage channels, and (b) the current channels.

4.2.2 Harmonic Current and Voltage Results

The approach adopted in the use of CHART was to record the average levels over a pre-defined time span (say one minute). From this data, trends in harmonic levels over time can be easily graphed by displaying harmonic voltage or current versus time, as illustrated in the results of Figure 4.4. This figure shows the average harmonic voltage and current levels for the RED phase over 10 second intervals. Shown beside each 'scratch' graph is a histogram, giving the occurrence of a particular harmonic voltage or current.

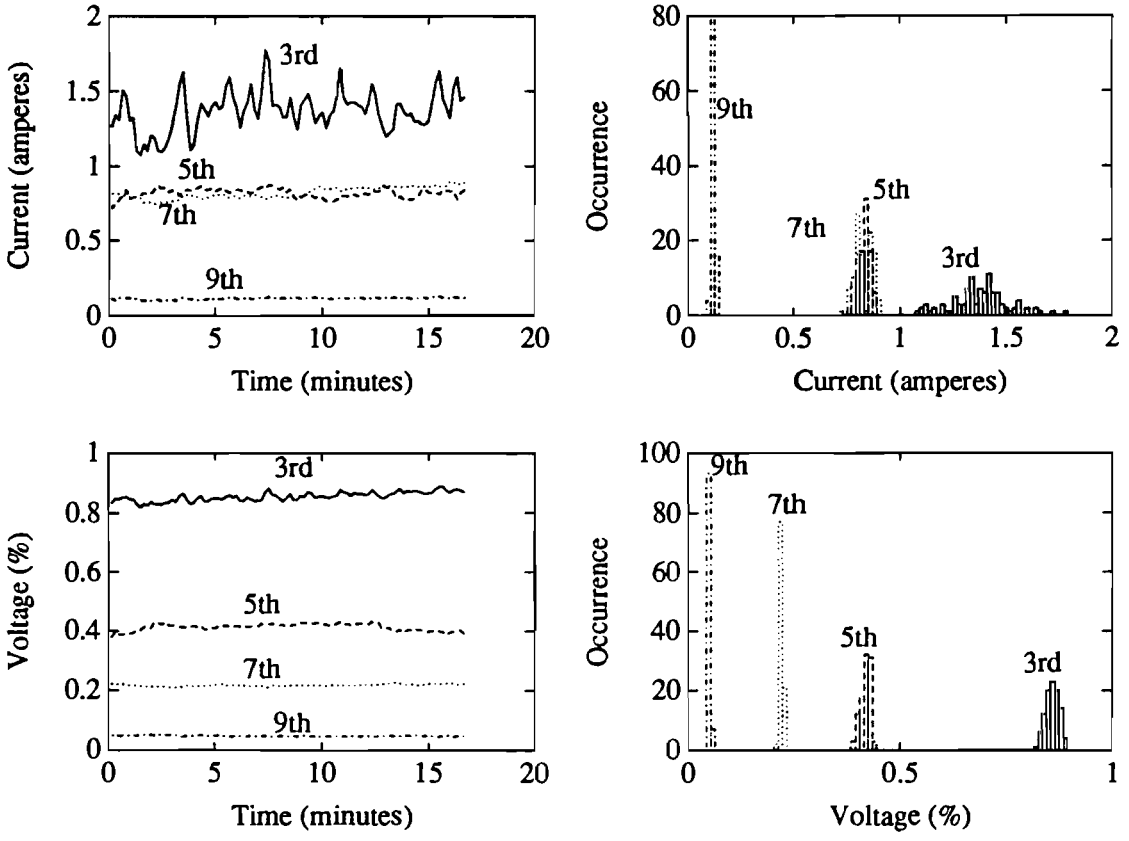


Figure 4.4 Selected red phase voltage and current harmonics measured at the Islington substation on the Islington-Twizel 220kV transmission line, beginning at 2pm, Thursday July 26, 1990. Current is shown in amperes and voltage is shown as a percentage of the nominal system phase to Earth voltage.

During monitoring, instantaneous harmonic magnitudes for all three phases up to the 50th harmonic can be displayed on a single chart, as illustrated in Figures 4.5 and 4.6. Readily apparent from the charts is that the blue phase 3rd harmonic voltage is significantly lower than that of the red and yellow phases, which illustrates the importance of three phase harmonic measurement and display.

4.2.3 Harmonic Impedance and Power

Harmonic impedance data of a supply system is of importance to supply authorities and consumers, as high harmonic impedance can indicate a possible resonant condition which could lead to the

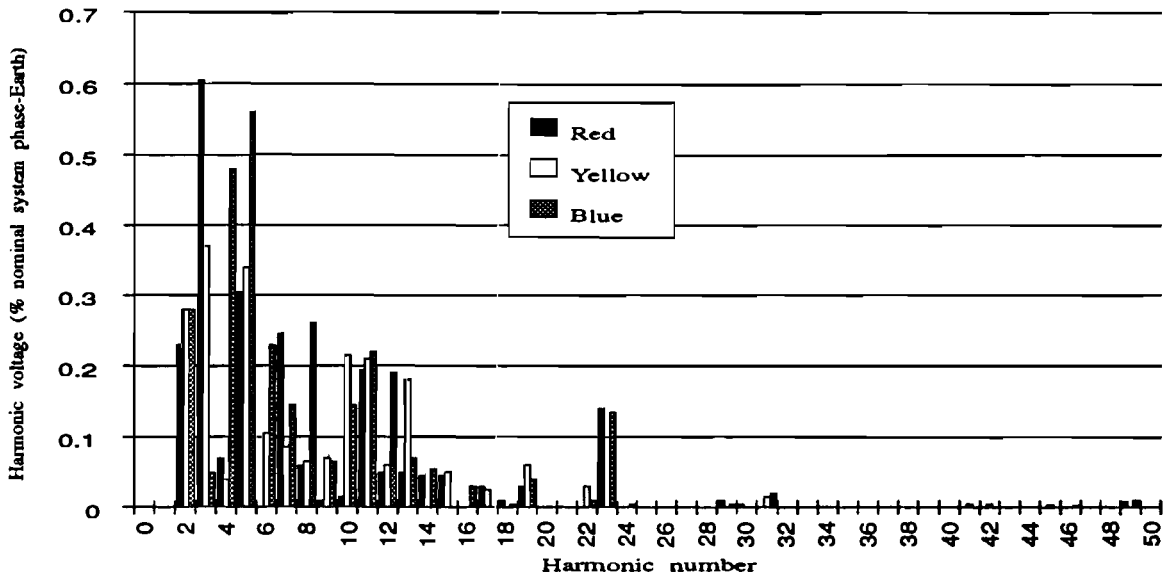


Figure 4.5 Harmonic voltages measured at the Islington substation on the Islington-Twizel 220kV transmission line, 1:30pm, Wednesday July 25, 1990.

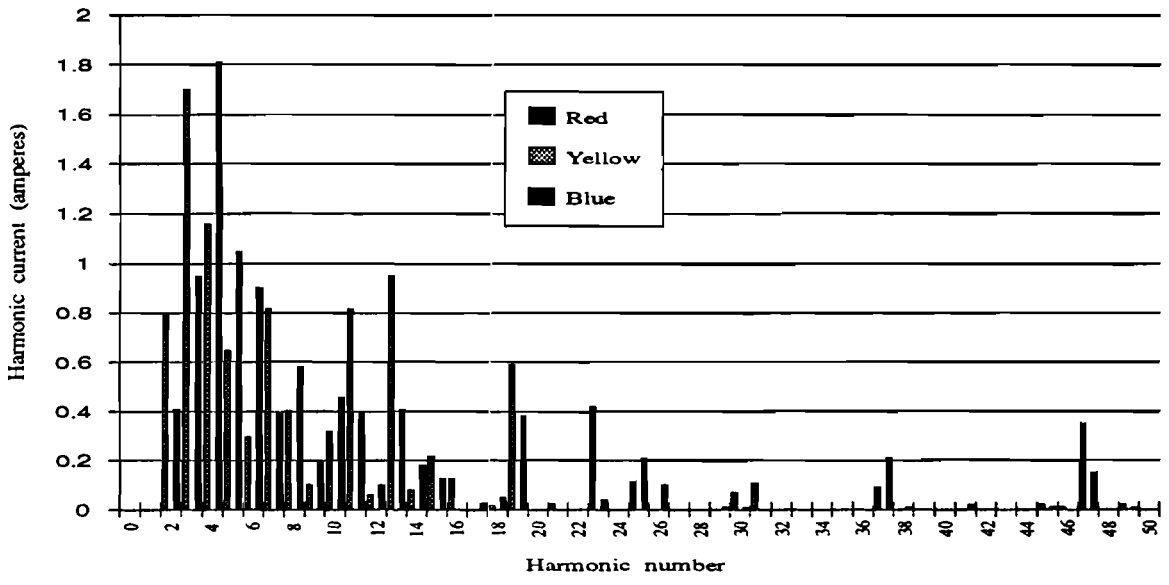


Figure 4.6 Harmonic currents measured at the Islington substation on the Islington-Twizel 220kV transmission line, 1:30pm, Wednesday July 25, 1990. Yellow phase current harmonics are not shown, as the signal representing yellow current was not available from Electricorp's equipment.

amplification of harmonic voltages. Given that the CHART harmonic monitor can compute harmonic voltage and current at a busbar (both magnitude and phase), it is possible for it to compute harmonic impedance at a busbar [de Oliveira *et al.*, 1989], given by

$$\tilde{Z}_n = \frac{\tilde{V}_n}{\tilde{I}_n} \tag{4.1}$$

or

$$\tilde{Z}_n = \frac{V_n}{I_n}\angle(\phi_{vn} - \phi_{in}), \tag{4.2}$$

where,

n is the harmonic order, V_n is the harmonic voltage magnitude resulting from the harmonic current $\tilde{I}_n$, I_n is the magnitude of harmonic currents in the line, and ϕ_{in} and ϕ_{vn} are the phase angles of $\tilde{I}_n$ and $\tilde{V}_n$ respectively.

Impedance obtained using equation 4.2 may not represent the impedance of a supply. This is certainly true if loads generating harmonic currents are present in the ac **supply** system while testing, and if the transducers used to provide voltage and current information are inadequate. Reliable measurement of an ac systems harmonic impedance in a non-invasive way is a difficult task requiring comprehensive investigation under a range of operating conditions, and the identification of all harmonic sources [Arrillaga *et al.*, 1985b]. Clearly the CHART system is capable of calculating harmonic impedance, although the results require careful interpretation.

To be able to measure harmonic impedance makes CHART an extremely valuable tool in the comparison of actual harmonic impedance with theoretically determined harmonic impedance, and in harmonic filter design. When used to make measurements over a long time span, CHART can determine regions of harmonic impedance for three phases, rather than single points corresponding to harmonics on an impedance locus. Results from CHART are not confined to harmonic frequencies; by analyzing voltage and current over as many as 16 cycles, frequencies to a resolution of almost 3 Hz can be resolved.

Active and reactive harmonic power in each phase can also be obtained from harmonic voltage and current, along with the direction in which they are flowing. This information could be useful in resolving harmonic problems by identifying sources of harmonic power. Since accurate magnitude and phase information is necessary for this measurement, reliable CTs and VTs must be used - the accuracy of CHART's results is dependent on it being used correctly.

4.3 Conclusion

This chapter has documented the use of an advanced harmonic monitoring system in the field. The prime benefit of these tests has been to provide guidance on the future development of the CHART system.

Given the nature of the algorithms used to compute harmonic levels and the number of channels required, multiple DSPs are ideally suited to this application. The increased processing power afforded by DSPs can lead to simplifications in data acquisition hardware and an improved signal to noise ratio in the acquired signal by oversampling voltage and current waveforms and filtering them using the DSP [Crochiere and Rabiner, 1983]. In addition to this, Multibus II in conjunction with Intel's multitasking real-time operating system (iRMX) forms a very powerful platform for multi-processing real-time systems. The tremendous number of features offered by the very highly integrated Multibus II CPU boards that Intel are now producing and the increased market acceptance of Multibus II means that a Multibus II based system is even more attractive than it was when the project began in 1986.

The reliance on existing analog fibre optical transmission links to transmit voltage and current signals to the main CHART unit was considered a major disadvantage in any harmonic monitor because the fundamental level cannot be measured reliably. When the project began in 1986, standard windowing environments for the development of the control and display software for the PC were not available. As a result of this, a custom windows environment was written as part of the project. Although this windows environment was very good, with the emergence of standard windowing software (such as Microsoft Windows) in the late 1980s it was decided to change from the custom software to a standard, which is supported by industry, and which is constantly upgraded.

This chapter has addressed a number of short falls of the CHART I system. Solutions to these problems are incorporated in the CHART II harmonic monitoring system which is the subject of the next chapter. The field tests outlined in this chapter have lead to the publication of a paper in the proceedings of the 1992 conference of the Institute of Professional Engineers New Zealand [Miller and Dewe, 1992a].

Chapter 5

THE CHART II HARMONIC MONITOR

5.1 Introduction

The previous chapter documented the use of CHART I in measuring harmonic levels at a substation. As a result of this exercise, and of visits by Mr. M.B. Dewe to the 1990 ICHPS conference in Hungary [Lake *et al.*, 1990] and of the author to the 1990 international iRUG conference [Miller *et al.*, 1990], a significant change to the CHART I system was conceived, leading to the superior CHART II system. Fundamental to the new concept was a shift from the analog fed multi-channel data acquisition system feeding a central processor, responsible for harmonic computation, to a modular system with processing power distributed amongst the data acquisition channels, and as close to the front end as practicable. Data acquisition and analog to digital conversion is performed in the switchyard next to 'bus gear', with converted data transmitted to the main processing unit by digital fibre optic cables.

By following this structure, and using the Texas Instruments TMS320C26 DSP, the new system has the ability to compute voltage and current harmonics for as many as 36 channels up to the 50th harmonic on a single Multibus II backplane. As in the case of CHART I, harmonics are computed for every fundamental cycle continuously and in real-time, and can be displayed as they occur. A major advance on CHART I is that the harmonic levels of each channel for every single cycle can be monitored on-line, leading to a significant reduction in required storage capacity and the ability to capture and store significant events.

The user interface to the instrument is by means of a custom designed application running under Microsoft Windows 3.1 on a 386/486 PC workstation running MSDOS 5.0. The PC communicates with the main processing unit using the TCP/IP protocol on an Ethernet link. The networked connection enables the workstation to be situated at a location other than that of the main CHART unit, and also enables multiple users to access CHART data by using different workstations. Multiple CHART units may be connected to the same network, and Ethernet communication facilitates the possibility of interconnecting to power system System Control And Data Acquisition systems (SCADA).

This CHART system incorporates a GPS satellite time referenced accurate real-time clock feature that enables the unit to accurately time stamp data acquired from power system transducers. This feature, combined with CHARTs ability to sample voltage and current signals at frequencies higher than those required by harmonic analysis, means that it is a powerful tool for use in transient

analysis of power system waveforms, and has found applications in fields such as fault location on transmission lines. Furthermore, by using several units at geographically separate locations on the same network, it has the inherent capability of enabling precise simultaneous measurement of power system parameters.

This chapter gives an overview of the CHART II system, covering topics such as its connection to current and voltage transformers on busgear, the parallel processing system and software used to compute harmonic levels, and the networked user interface to the system. It also covers the development of hardware and software for CHART II from its initial conception in November 1990 to the use of a prototype to make measurements in October 1992. Photographs of various CHART II system components are included in Appendix 5C.

5.2 An Overview of CHART II

The CHART II system is illustrated in figure 5.1. It consists of three main sections: The multiple remote data conversion modules (RDCMs), a parallel processing system, and a network of workstations.

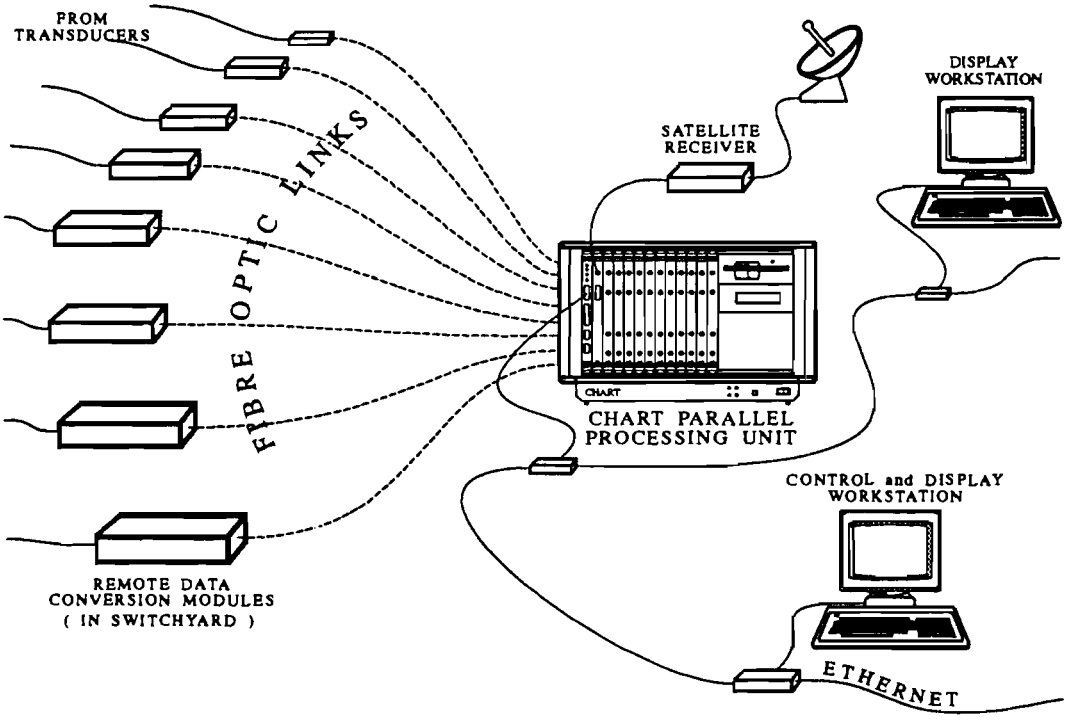


Figure 5.1 The CHART harmonic monitoring system.

As depicted in figure 5.1, each analog voltage signal, representing either voltage or current, is converted to a digital representation by the remote data conversion modules and transmitted to the parallel processing system by fibre optic cable. This isolates the computer equipment and users from potentially hazardous voltages developed under fault conditions in a switch yard. The use of optical links between the conversion modules and the processing system also eliminates the

problem of ground loops and the resultant noise in the instrumentation system, as well as other electromagnetic coupling.

The parallel processing system is responsible for the computation of harmonic levels in the signals received from the RDCMs, and for monitoring the levels. It also handles communication of data to display workstations, and storage of harmonic data. The configuration of the parallel processing system, and the display of harmonic levels, is handled by PC workstations running Microsoft Windows. The CHART II system and the workstations are networked on Ethernet, which is used with TCP/IP to communicate data between the parallel processing system and the workstations.

5.2.1 Remote Data Conversion Modules

The remote data conversion modules are used to convert current transformer and voltage transformer outputs to 16 bit digital signals, and to transmit them to the processing system. The RDCMs are typically located next to busgear (either interior or exterior), near the current and voltage transducers to which they are connected. They receive their analog to digital conversion command from the parallel processing system (via a fibre optical cable), thereby ensuring that conversion occurs simultaneously on each channel. Sampling is synchronous with the power system fundamental as discussed in Section 6.2.2. In a specific application, consideration must be given to propagation delays in the fibre optic links if sampled data is to be time stamped accurately. Each RDCM is a stand-alone module, powered independently by batteries[1], trickle charged by a mains power supply if desired. Solar panels, may be added to trickle charge the batteries, which would avoid the running of power leads between units in a monitoring environment, and which would also enable a high degree of freedom of placement of the modules when connecting CHART to a power system. Alternatively the RDCM units can be powered by a common supply. This in turn enables a large amount of flexibility in monitoring various points on a power system. Separating the RDCMs from the main processing unit facilitates the tailoring of the analog/digital conversion circuitry to particular application requirements in a functional and cost effective way. The structure of a typical RDCM is outlined in Figure 5.2.

5.2.2 The CHART Parallel Processing System

The CHART parallel processing system is based on the Intel Multibus II bus architecture and uses the Intel Real-Time Multitasking operating system, iRMX386 release III.3, to schedule the tasks required to collect, store, and distribute data. Harmonic levels in the signals acquired from the RDCMs are computed using FFTs [Brigham, 1974], which is a computationally intensive process. For this reason, processing in the CHART system has been distributed over multiple DSP cards and moved as close as practicable to the front end data acquisition stage. The general structure of this is illustrated in Figure 5.3.

Multiple data acquisition and processing cards or modules (DAPMs) are arranged to acquire and process two channels of data each, giving a total of 2n channels (where n is the number of

[1]The battery capacity of each RDCM enables up to 5 days of continuous operation before recharging is required

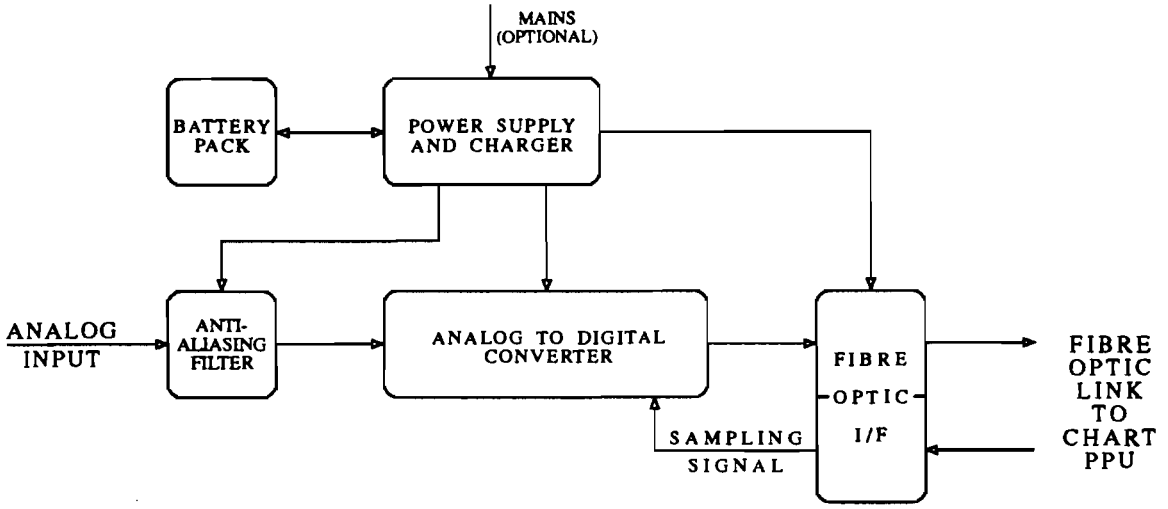


Figure 5.2 A remote data conversion module.

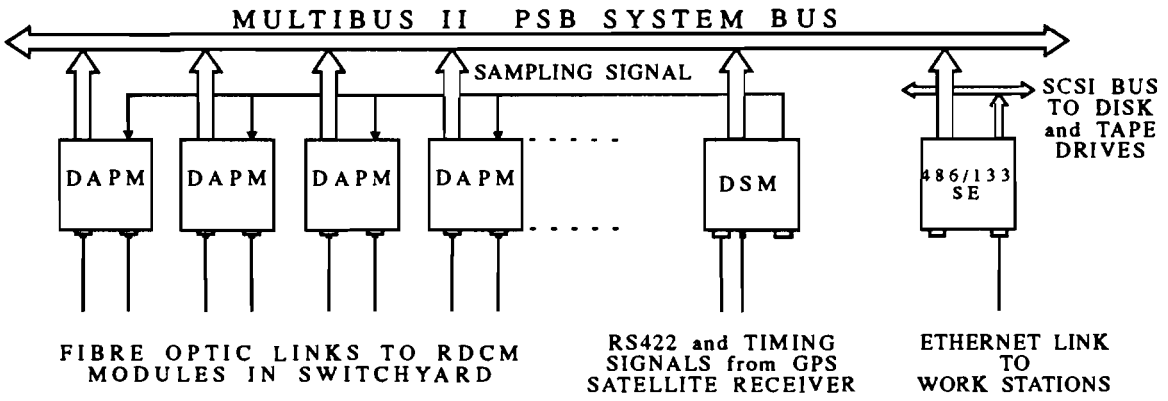


Figure 5.3 The CHART parallel processing unit.

DAPMs). These cards incorporate a full interface to the Multibus II PSB, and are capable of message passing their results to any other card on the bus. However, as illustrated in figure 5.4, the system software is arranged so that the 486/133SE card acts as a central collection point for the DAPM results, and also performs any further computation required. If the computation required is too great for the 486/133SE card, it can 'farm' computation out to other processor cards added at a later stage as the system expands. This illustrates the importance of a good multiprocessing bus - one of the advantages of Multibus II is that extra processor cards can be added with minimal effort and with no fundamental hardware changes.

The final card in the central processing system is the Digital Services Module (DSM) whose functions are twofold. Firstly it provides accurate timing and fundamental frequency information to the 486/133SE card for time-stamping of acquired data, and secondly, it produces sampling and synchronization signals for the data acquisition stage. The DSM monitors the power system fundamental frequency and produces a sampling signal that is exactly 1024 times the frequency of the fundamental. Sampling of voltage and current is therefore coherent, and spectral leakage [Brigham, 1974] from the FFT is minimal, as discussed in Section 6.2.2. Because spectral

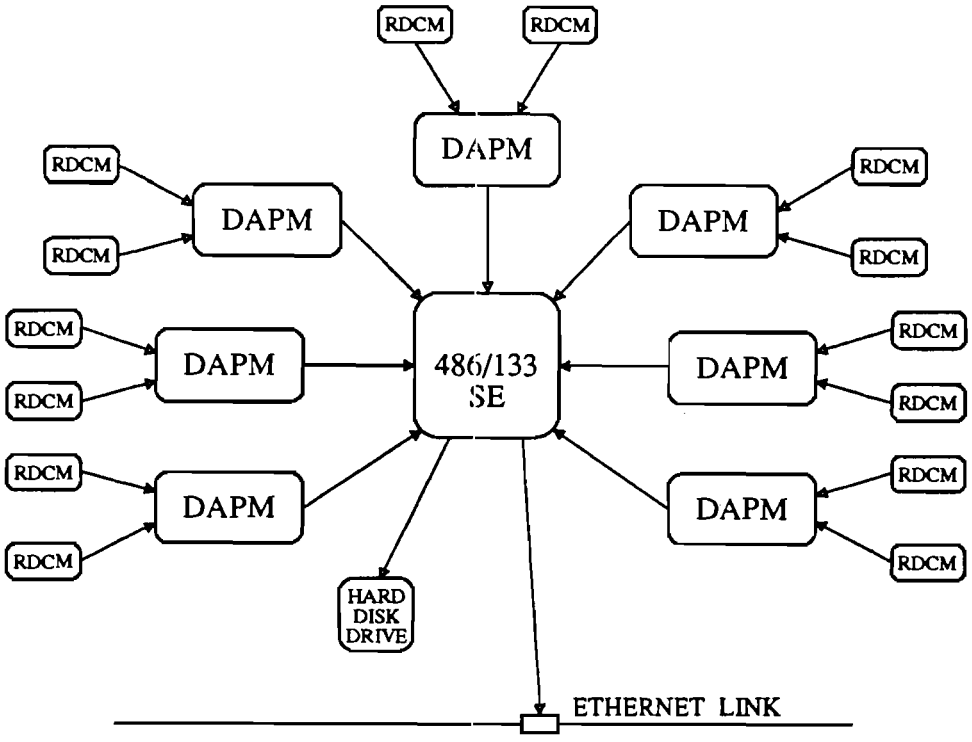


Figure 5.4 Data flow in the CHART parallel processing system. The 486/133SE computer acts as a central collection point for DAPM data.

leakage is minimized by coherent sampling, the added computational burden of windowing the input data is not required. The device used to produce a coherent sampling signal is the SRM which is discussed in section 5.2.2.3. The DSM can also produce a sampling signal of fixed frequency if selected by a user, and can produce a sampling signal of 102.4/112.88 kHz for transient analysis of 50/60 Hz systems. A GPS satellite receiver interface is incorporated into the DSM to enable it to receive very accurate timing information. This time is latched by the sampling signal and matched with captured data by the 486/133SE computer. The DSM communicates timing data to the 486/133SE over the Multibus II PSB. Even higher sampling rates are possible (in the order of 1MHz) with the appropriate RDCM design.

The maximum number of channels that can be monitored by the CHART system is limited by three factors. Firstly the number of available slots on the Multibus II backplane, secondly the processing power required to process the extra data, and finally limitations of the iPSB bus bandwidth. The largest Multibus II backplane has 20 slots, and with one 486/133SE and one DSM, 18 are left free for DAPMs. The extra processing requirements for harmonic analysis are added to the system automatically as more channels are added, in the form of DAPMs, which perform the FFT processing and on-line monitoring. The PSB bus can support a sustained transfer rate of 10 million transfers per second. When configured for harmonic analysis, the combined transfer rate for 19 DAPMs is less than 1 Million transfers per second, which is the maximum required for this particular application. Bus bandwidth and processing power would however be limiting factors with the significantly higher sampling rates used by transient analysis, although

it is anticipated that the front end DSPs would be used to operate on transient data, reducing its rate. As part of the on-going development of Multibus II by Intel, its bandwidth has been doubled recently by doubling the bus clock frequency. This opens possibilities for higher sampling rates in future applications.

5.2.2.1 Data Acquisition and Processing Modules

(a) Introduction

Each DAPM incorporates a fibre optic cable interface, and can acquire raw time domain data (in a serial digital format) transmitted from two independent RDCMs. As depicted in figure 5.5, two Texas Instruments TMS320C26 DSPs (one for each channel) are used to process the acquired data. The DSP results are stored in FIFO buffers for transfer to the 80186 micro-computer. The 80186 micro-computer handles all message transactions over the Multibus II PSB via the MPC bus interface unit. The DAPM card supports interconnect space - a feature of Multibus II that allows centralized control and coordination of all cards identification, configuration , and diagnostics, as discussed in Appendix 5A.

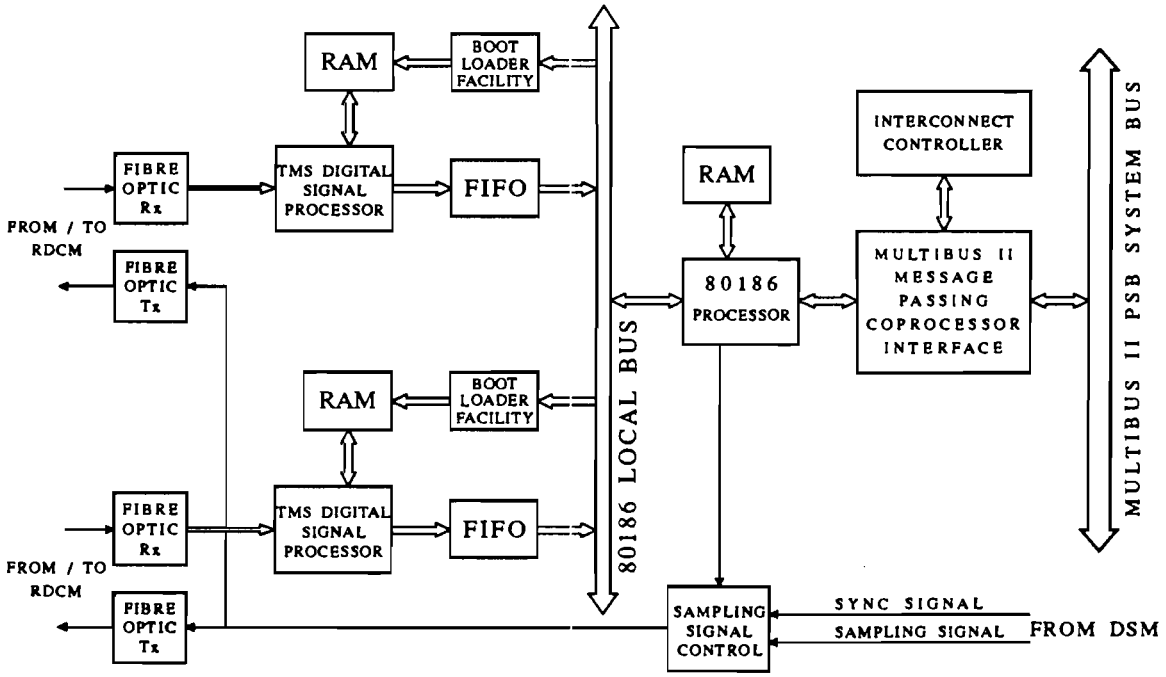


Figure 5.5 Data acquisition and processing module structure.

(b) The TMS320C26 Fixed Point Digital Signal Processor

The TMS320C26 is a member of the family of Texas Instruments fixed point very large scale integration digital signal processors. It is identical to the TMS320C25 DSP [TI, 1986] in design

but has a larger internal RAM. The internal architecture of the TMS320C26 is a 32-bit Harvard type in which program and data memory reside in separate address spaces, allowing a full overlap of instruction fetch and execution. Externally the program and data memory are multiplexed over the same 16-bit bus so as to maximize the address range for both spaces while minimizing the pin count of the device. Other features of the device are:

- 100ns instruction time.
- 1568 words of configurable on-chip program/data RAM.
- TMS320C25 object code compatible except for RAM configuration instructions.
- 256 words of on-chip program ROM.
- 128 kwords of data/program space.
- Sixteen input and sixteen output channels.
- 16-bit parallel interface.
- Directly accessible external data memory space.
- Global data memory interface.
- 16-bit instruction and data words.
- 32-bit Arithmetic Logic Unit (ALU) and accumulator.
- Single-cycle multiply/accumulate instructions.
- 0 to 16-bit scaling shifter.
- Bit manipulation and logical instructions.
- Instruction set support for floating point operations, adaptive filtering, and extended precision arithmetic.
- Block moves for data/program management.
- Repeat instructions for efficient use of program space.
- Eight auxiliary registers and dedicated arithmetic unit for indirect addressing.
- Serial port for direct codec interface.
- Synchronization input for synchronous multiprocessor configurations.
- Wait states for communication to slow off-chip memories/peripherals.
- On-chip timer for control operations.
- Three external maskable user interrupts.

- Input pin polled by software branch instruction.
- Programmable output pin for signalling external devices.
- CMOS technology.
- Single 5V supply.
- On-chip clock generator.

The dynamic range of the signals acquired by the CHART RDCMs is 16 bits, which enables 16 bit fixed point arithmetic to be used in the anti-aliasing filter and FFT. The use of floating point arithmetic was considered, although the relative hardware simplicity of the fixed point TMS320C26 versus floating point DSPs (namely the TMS320C30) was considered more of an advantage than the slightly more complicated software involved in a fixed point implementation. In any implementation, be it fixed or floating point, a clear understanding of the number representation and arithmetic is essential. This understanding reduced the seemingly more complicated fixed point implementation to quite a simple problem. Other issues involved in the decision to use fixed point arithmetic are that integer number representation is standard amongst different processors, whereas real number representation varies between different manufactures. Furthermore, integer representation is more efficient (requiring only 2 bytes of storage as opposed to 4 for real numbers), which is important for achieving maximum throughput on limited bandwidth channels, and naturally requires less storage. The TMS320C26 was used (as opposed to the TMS320C25) because of its larger internal RAM, in which the FIR filter and FFT are implemented at a higher speed than external RAM because of the internal 32-bit Harvard-type architecture of the TMS320C26. The Texas Instruments family of DSPs was used simply because considerable expertise exist within the department of Electrical and Electronic Engineering with this family, and because the software development tools were readily available. Further information about the TMS320C26 can be found in [TI, 1991].

(c) DSP Executable Down-Loading and DAPM Control

Each DSP has 64 kwords of external static RAM, divided into 32 kwords of program RAM and 32 kwords of data RAM. This amount of external data RAM enables the DSPs to buffer data when sampling at higher sampling rates for transient analysis. A DMA facility from the 80186 microcomputer to the DSPs program RAM is provided. Hence an image of a program that a DSP is required to execute can be placed directly into its program RAM by its host 80186. Software operating on the 80186 is able to receive this program image over the PSB from the 486/133SE computer. As well as acting as a boot server, the 486/133SE acts as a file server, storing DSP executables received from a PC workstation, via Ethernet, where they are developed using the Texas Instruments fixed point DSP software development tools.[2] When instructed by

[2]As explained in the Conclusion to this chapter, the TCP/IP software for the 486/133SE computer is unavailable at present, meaning that a complete Ethernet interface is not possible. Hence a temporary means of transferring files between a PC and the 486/133SE file server using a floppy disk is used, as illustrated in Figure 5.6.

the 486/133SE, the host 80186 can boot the DSPs to begin their program execution. This is usually done by the 80186 releasing the reset on the DSP, and subsequently enabling the sampling signal to pass to its RDCM. All DAPMs are instructed to do this simultaneously by broadcasting an unsolicited message from the 486/133SE computer to a port on all boards in the Multibus II system (the details of ports and broadcast messages are covered in Appendix 5A). This boot-loading process is illustrated in Figure 5.6. The ability to download bootable program images to the DSPs from a workstation is a key feature of CHART II, giving it tremendous potential as a research tool, as well as a power system instrument. Using this feature, CHART can be used for a variety of functions such as harmonic analysis over any number of cycles of the fundamental, or fault detection. The analysis technique used is selected by the user at a workstation from a number of options. The appropriate bootable image is then downloaded to the appropriate DSP, taken from a collection of pre-compiled DSP programs corresponding to each option.

(d) DAPM Processing Algorithms and Data Flow

For harmonic analysis, voltage and current waveforms are sampled at eight times the frequency required to resolve up to the 50th harmonic. Oversampling in this manner reduces the complexity of anti-aliasing filters in the RDCMs and leads to an improved signal to noise ratio in the sampled signal as discussed in section 6.2.2. The sampling signal is generated on the DSM and sent via each DAPM to the RDCMs. The DAPM can gate the sampling signal to each RDCM independently if data from that channel is not required. A data flow diagram illustrating an example of the data flow rates and processing performed by a DSP for harmonic analysis is shown in Figure 5.7. Acquired data is passed through an 8:1 decimation anti-aliasing finite impulse response filter [Crochiere and Rabiner, 1983]. This reduces its rate to precisely 128 samples per 50 or 60 Hz cycle. The FIR filter output is averaged over 4 cycles[3] and placed in a FIFO buffer as well as being passed to an FFT routine. This performs an FFT on data accumulated for one averaged cycle, and places the output data in a second FIFO buffer. Obviously for the DSP to perform FFTs continuously on a cycle by cycle basis, data must be buffered, which is another reason for the DSPs external data RAM. Data flow and buffering in the DSP is discussed in Section 6.5. The 80186 microcomputer reads the time domain data and harmonic information from the FIFOs and monitors it, sending results to the 486/133SE computer. In this way all of the processing that is required on the captured data (namely harmonic computation and on-line monitoring) is performed by the DAPMs, making it very simple to extend the capabilities of the system to monitor additional channels by adding extra DAPMs. This makes full use of the 80186 microcomputer on the DAPMs which is required for the complete Multibus II interface, but which only spends a small proportion of its time dealing with that interface.

Any compensation for transducer characteristics can be easily performed in the frequency domain by the DSPs. One of the planned additions to CHART is a data base of standard current transformer and voltage transformer characteristics.

[3]Averaging over 4 cycles is used to comply with New Zealand legislation (discussed in Section 2.2.3.3). Averaging is only one option - longer FFT record lengths can be used instead as illustrated in Figure 5.7.

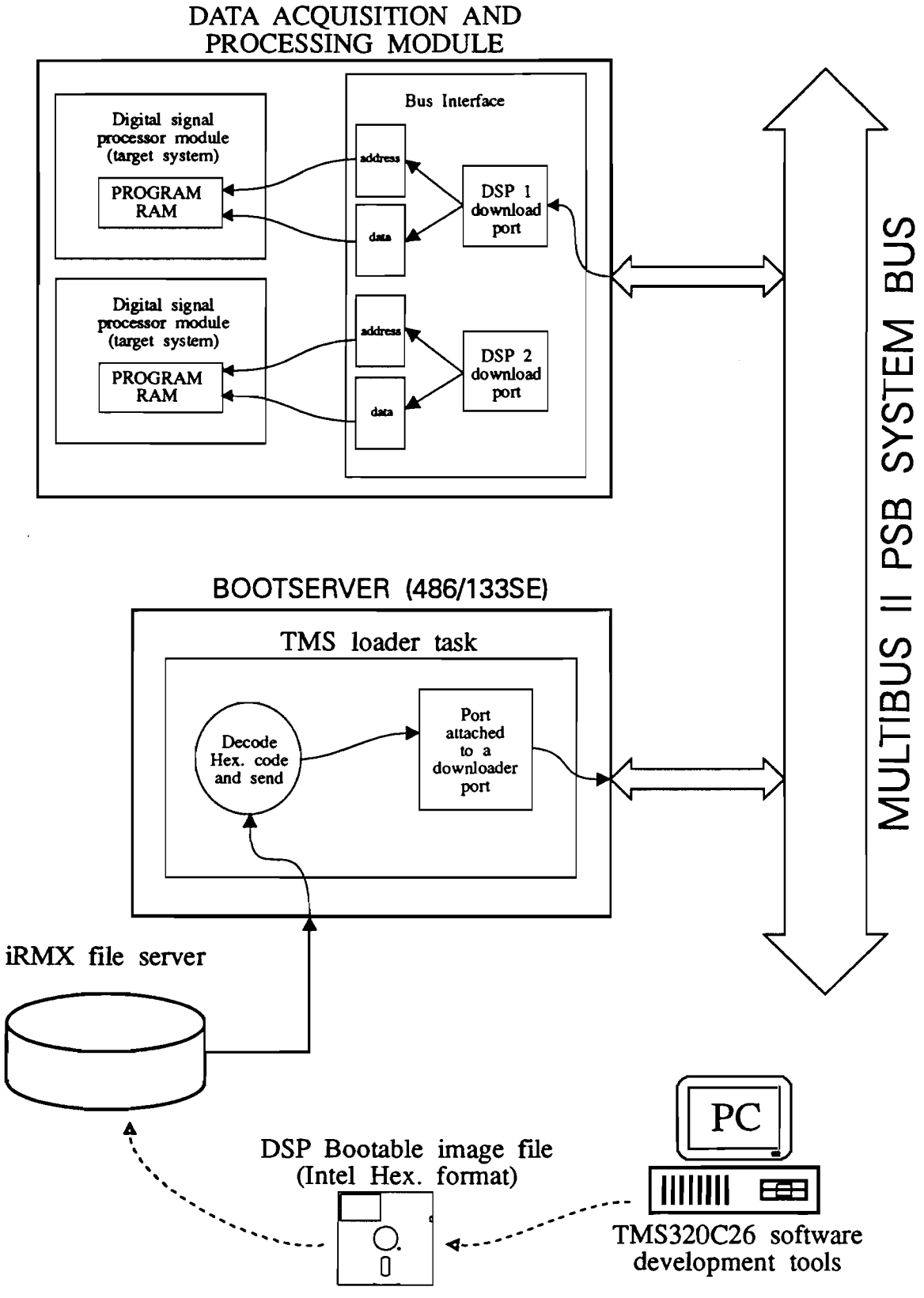


Figure 5.6 Development of DSP executables on a PC and downloading to the program RAM of a DSP.

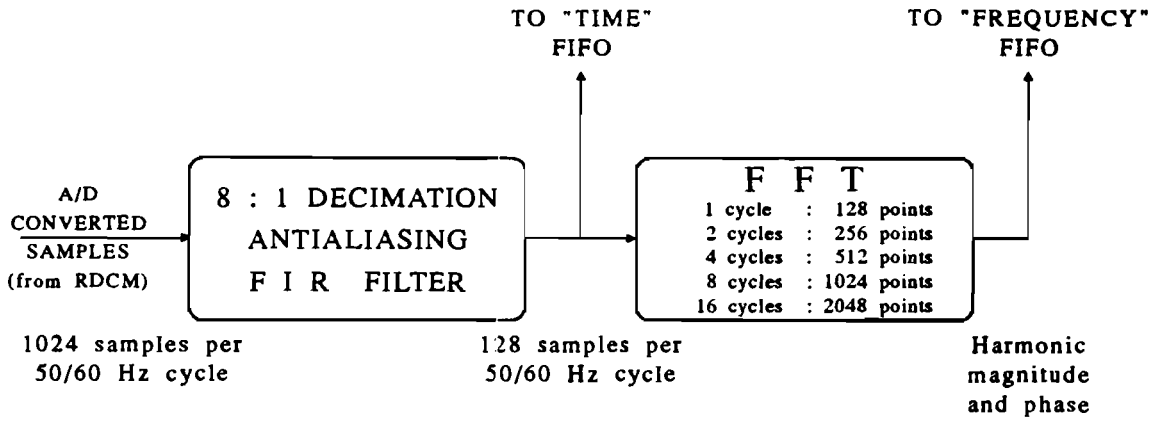


Figure 5.7 Data flow and processing for harmonic analysis.

5.2.2.2 The 486/133SE Computer

As discussed in the introduction to this section, the CHART processing system software is arranged so that the 486/133SE single board computer acts as a central collection point for the data from all of the DAPMs after it has been passed through a suitable on-line monitoring algorithm on a DAPM. The 486/133SE card is a highly integrated Intel single board computer that incorporates an 80486 micro-processor with internal cache RAM and coprocessor operating at 33 MHz, 16 Mb of dynamic RAM, a full Multibus II interface, a Small Computer Systems Interface (SCSI) protocol controller for interfacing to disks, a DMA controller, several serial Input/Output (I/O) controllers, and a Local Area Network (LAN) coprocessor for interfacing to Ethernet. This computer acts as a client in the client/server model discussed in Appendix 5A, receiving harmonic information and time domain data from DAPMs. It also acts as a disk server by storing and retrieving harmonic information and DSP executables, and a communication server, interfacing the processing system to workstations on Ethernet.

The principle behind the operation of this board is that only data required 'down stream' for further processing, or for storage or display by a workstation is obtained from a DAPM. Hence the Multibus II resources are not tied up handling unwanted data. Each DAPM can be viewed as a data server, supplying the following data:

- Time domain data from DAPM channel A
- Frequency domain data from DAPM channel A
- Time domain data from DAPM channel B
- Frequency domain data from DAPM channel B

Multiple DAPMs provide an array of data for the multiple channels, with each DAPM uniquely addressable over Multibus II.

If a particular DAPMs data is required by some task operating on the 486/133SE computer (a communication task to a workstation for instance), a requesting task for that data is created

and attached to the socket representing the DAPM. It then requests the data, and when received from the DAPM (in the form of a standard packet using a solicited message transaction), stores it in a file on the hard disk connected to the 486/133SE SCSI port. This file is used as a means of communicating harmonic data from one task to another.[4] Various methods were investigated, such as mailboxes and short circuit messages. Using a mass storage device to pass data between jobs in this fashion is seen as a 'last resort' in RMX systems. However in this application it was considered the most appropriate, as data is stored on the hard disk anyway, and it leads to very simple code. Additionally this completely decouples the data storage and retrieval jobs, enabling the storage task to be run as a background task, while the retrieval task can be run in foreground mode. This data flow between tasks is illustrated in Figure 5.8.[5] Solicited message transactions over Multibus II are covered in Appendix 5A.

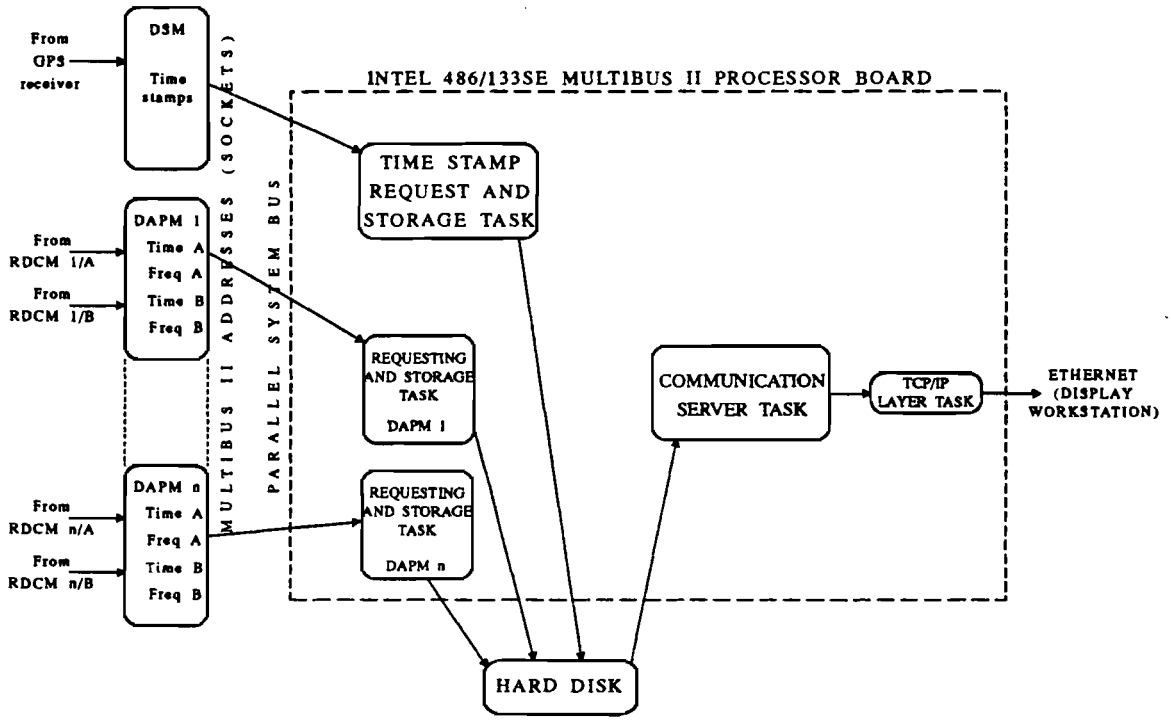


Figure 5.8 An example of multiple tasks operating on the 486/133SE computer.

The 486/133SE computer runs the iRMX operating system which schedules the various tasks. It also handles bootloading of the DAPM software during the boot phase of the system operation [Miller *et al.*, 1990], and incorporates Multibus II central service functions that provide system level services to all of the DAPMs [Mahoney, 1990]. Appendix 5A covers iRMX and Multibus II concepts employed in the CHART project.

[4]Data requested by the display system is retrieved from the hard disk by a communication server task. Because data is only stored once every 10s, the harmonic display can only be updated at this rate. A faster method of data transfer to the display system will be implemented once the Ethernet connection is completed.

[5]As explained in the Conclusion to this chapter, the TCP/IP software for the 486/133SE computer is unavailable at present, meaning that a complete Ethernet interface is not possible. Hence a temporary means of transfering data to display workstations using a spare serial port on the 486/133SE is used.

5.2.2.3 The Digital Services Module

The Digital Services Module (DSM) is based on the same Multibus II interface as the DAPMs (an 80186 microcontroller and message passing co-processor), and incorporates two units. These are the Real-Time Clock (RTC) and Sample Rate Multiplier (SRM). The real-time clock has a GPS satellite receiver interface to enable precise time stamping of data, as well as an interface to fault detection transducers for fault location on HVdc lines. The RTC is still under development as a masters project for HVdc fault location [Dewe *et al.*, 1992].

(a) The Sample Rate Multiplier

As discussed in Section 3.3.1, the CHART I SRM adjusts the analog to digital conversion sampling interval to maintain it at an 'exact' $\frac{1}{128}$ sub-multiple of the fundamental period. In effect it accommodates the small changes that may occur in the mains frequency which can cause spectral leakage from the FFT as discussed in Section 6.2.2. The SRM employed by CHART II is identical in concept to that used in CHART I, but is designed to maintain the sampling interval at an exact $\frac{1}{1024}$ sub-multiple of the fundamental period. This is because CHART II over-samples voltage and current signals by a factor of 8 (as discussed in Section 6.3), resulting in 1024 samples per fundamental period.

The SRM is essentially a digital frequency-locked-loop, which multiplies the input frequency by 1024. A simplified functional block diagram of the SRM is illustrated in Figure 5.9. The concept of the SRM is straight forward, although its implementation was technically difficult, as it involved high speed counters and precise timing of logic signals.

The high speed counter illustrated in Figure 5.9 counts from an initial count set by the micro-controller to its terminal count (0FFFFh), after which it immediately rolls over to the initial count and begins counting again. This continuous action produces the sampling signal, which is sent to the RDCMs, as well as being fed back to the micro-controller. The micro-controller also receives a logic signal corresponding to the zero crossings of the fundamental frequency. Using this signal it counts the number of sampling pulses that occur in the fundamental period, and adjusts the initial count to the counter to give 1024 samples per cycle.

There are two issues associated with the SRM. These are the accuracy with which it can match the incoming fundamental period, which is a direct trade-off with the speed at which it can track the changing fundamental period as illustrated in Figure 5.10. The software operating on the micro-controller is designed to make the SRM a highly damped frequency locking device. The reason for doing this was to prevent the SRM from tracking very fast changes in fundamental frequency which may occur during transients on the power system, or which may originate from 'jitter' on the fundamental period zero crossings, which can be caused by noise. The highly damped response was achieved by simply modifying the counters initial count by one for each fundamental period, instead of estimating how much to adjust the counter's initial count based on how far off the output sample count is from the nominal 1024 samples per cycle.

The accuracy with which the SRM can match the incoming fundamental frequency is deter-

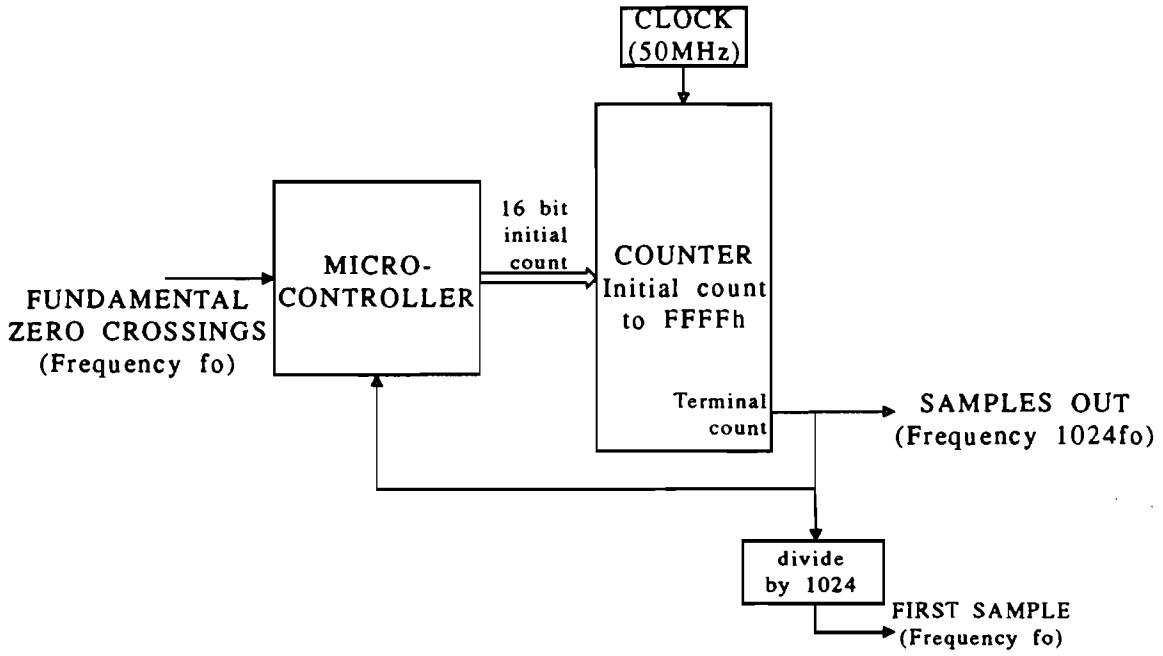


Figure 5.9 A simplified functional block diagram of the sample rate multiplier.

mined by the clock frequency, f_{clk}, and is given by

$$\Delta f \simeq \frac{1024(50)^2}{f_{clk}} \text{ Hz} \tag{5.1}$$

for a 50 Hz system. This is essentially the accumulation in error over 1024 samples caused by the initial count to the counter changing by 1. It is important to note that this is the accuracy of the sampling signal divided by 1024 (which is nominally 50 Hz), and not of the actual sampling signal which is 51.2 kHz. The derivation of Equation 5.1 is given in Appendix 5B.

The speed at which the SRM can track the changing fundamental period is the amount by which the frequency can be changed per 50 Hz cycle multiplied by 50. The amount by which the frequency can be changed per 50 Hz cycle is the accuracy of the SRM given by Equation 5.1. The SRM tracking speed is therefore

$$S_{SRM} \simeq \frac{1024(50)^3}{f_{clk}} \text{ Hz per second.} \tag{5.2}$$

Figure 5.10 depicts the SRM accuracy and tracking speed for various clock frequencies. Although the New Zealand Electricity Corporation gives no code of practice for the rate of change of frequency during load shedding, it is generally accepted that the absolute maximum rate of change of frequency on the New Zealand system is 2.5 Hz per second. From Figure 5.10, for the SRM to meet this requirement, f_{clk} must be below 50 MHz. To obtain maximum accuracy from the SRM, f_{clk} must be as high as possible. CHART II uses a 50 MHz SRM clock which gives it an accuracy of approximately 0.05 Hz from Equation 5.1. From Section 6.2.2 it can be seen that this accuracy is sufficient to stop significant spectral leakage from the FFT.

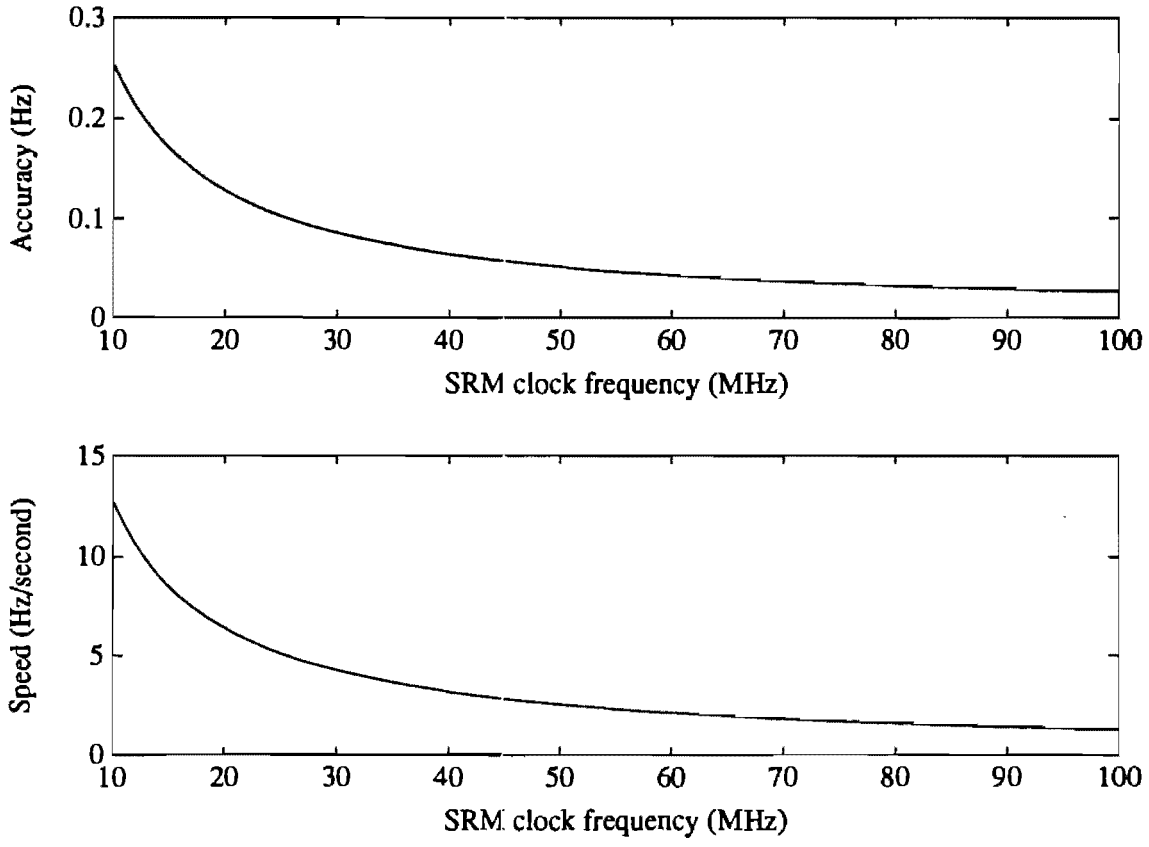


Figure 5.10 The trade-off between accuracy and tracking speed of the SRM.

(b) The Real-Time Clock

The RTC is a precise clock synchronized once a second, via a GPS satellite receiver, to a very accurate global time maintained by the GPS satellite system [Livingstone, 1992]. The initial time of the RTC is set by the GPS receiver through a serial connection between them, while the one second timing pulse is a dedicated signal.

Accurate time stamping of acquired data is achieved by latching the RTC time on the *first sample pulse* of each fundamental cycle. The first sample pulse is the SRM sample output frequency divided by 1024. It is used to synchronize each DAPM, so that after they receive a broadcast message instructing them to begin sampling, they all sample simultaneously, beginning from the first sample.

Each DSP maintains a cycle number counter, driven by the incoming samples which are synchronized to the first sample. The DSM CPU also maintains a cycle number counter, started by the 'begin sampling' broadcast message to DAPMs, and driven by the first sample pulse. Each time this cycle number counter is updated, the RTC latched time is read and sent with the counter to the 486/133SE computer. This computer time-stamps the DAPM output data that it receives by matching the DAPM data's cycle number counter with the equivalent counter from the DSM and appending the corresponding RTC time to the DAPM data. The principle of time stamping is illustrated in Figure 5.11.

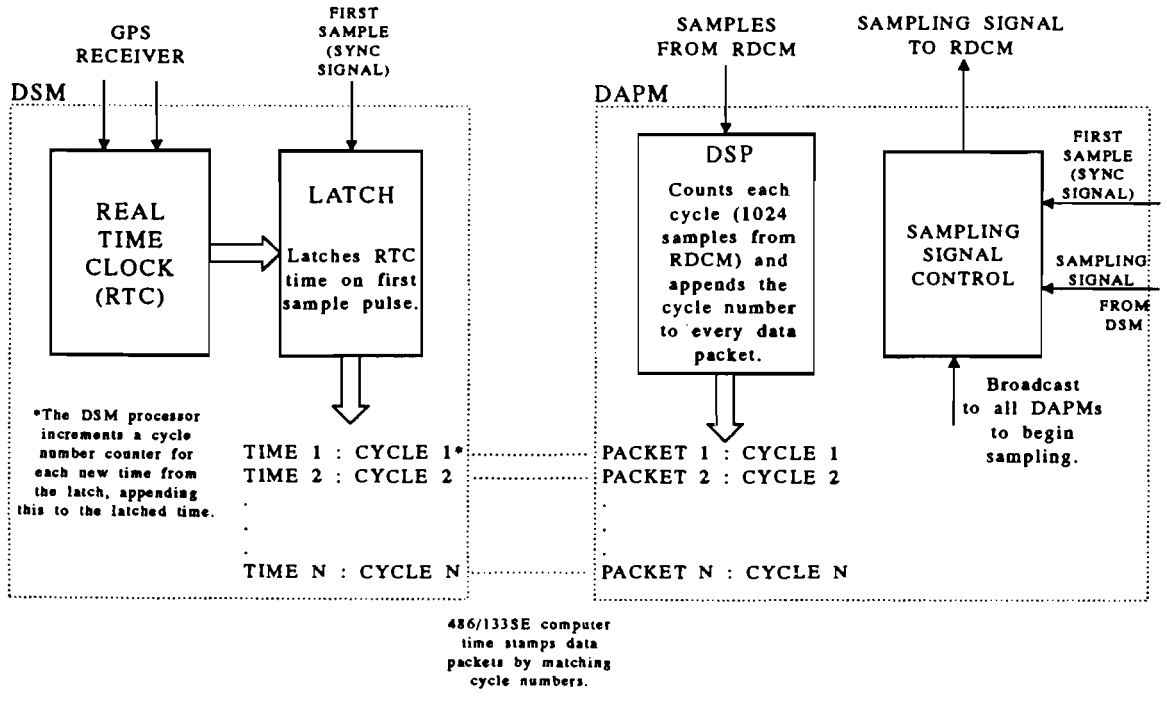


Figure 5.11 Precise time stamping of DAPM data.

5.2.3 CHART Control and Display Workstations

The display of power system voltage and current waveforms and of harmonic data is accomplished with custom designed application windows running under Microsoft Windows 3.1 on 486 PC workstations running MSDOS 5.0. The various data types are displayed on windows which are selected using a mouse and icons. Windows can be moved about the screen and scaled to any desired size. Multiple windows can also be displayed, with data in each window updated every 10 seconds.[6] Various displays are possible, such as magnitude versus harmonic number, voltage (per unit) and current (amperes) versus time, and magnitude for particular harmonics versus time. Figure 5.12 shows a typical display from CHART.

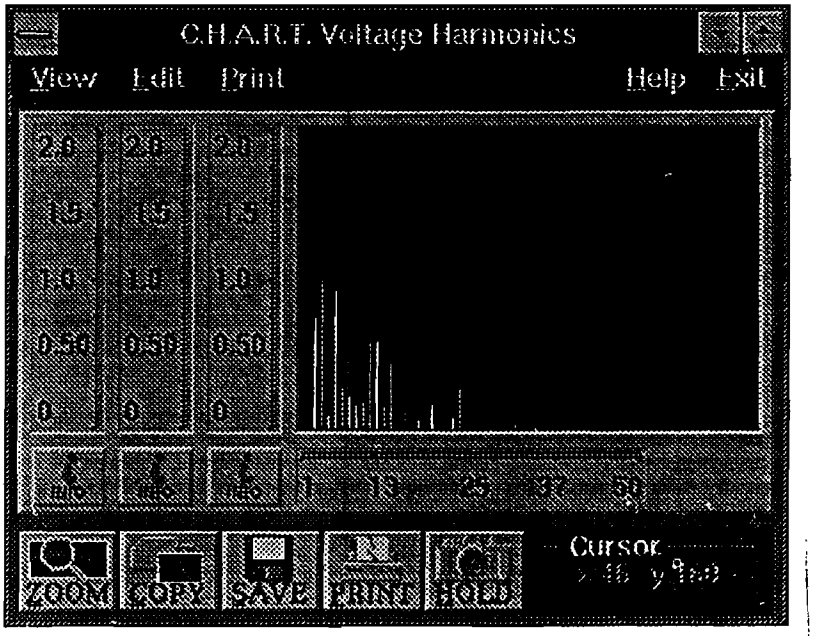


Figure 5.12 An harmonic display on the CHART user interface.

Ethernet is used as the physical communication path between display workstations and the CHART parallel processing unit. The protocol TCP/IP is used as the software layer on Ethernet, providing the CHART unit with a suite of standard applications such as FTP and TELNET. Actual harmonic data and time domain waveforms that are to be displayed are sent from the parallel processing unit to display workstations using TCP/IP sockets. Only one workstation in the network environment can modify CHART parameters - the control and display workstation. Telnet is used by this workstation to remotely log a user into the parallel processing unit (server). The user can then configure the CHART system for monitoring. This involves: naming channels, entering system parameters such as the nominal voltage, current and voltage transformer ratios, and the system frequency (50 or 60 Hz), selecting the sampling source (fixed or synchronized to the fundamental), and selecting the method of harmonic analysis (essentially whether the FFT should be computed over 1, 2, 4, 8, or 16 cycles). An example of the main display terminal on

[6] As explained in Section 5.3, a temporary serial connection to the display system is used which, because of its bandwidth limitations, effectively limits the display update rate. When the complete Ethernet connection to the display workstations is implemented, the update rate will be approximately once a second.

the control and display workstation is shown in figure 5.13. Display workstations essentially have read only access to chart data. Users at these workstations can view CHART data, but cannot modify CHART settings.

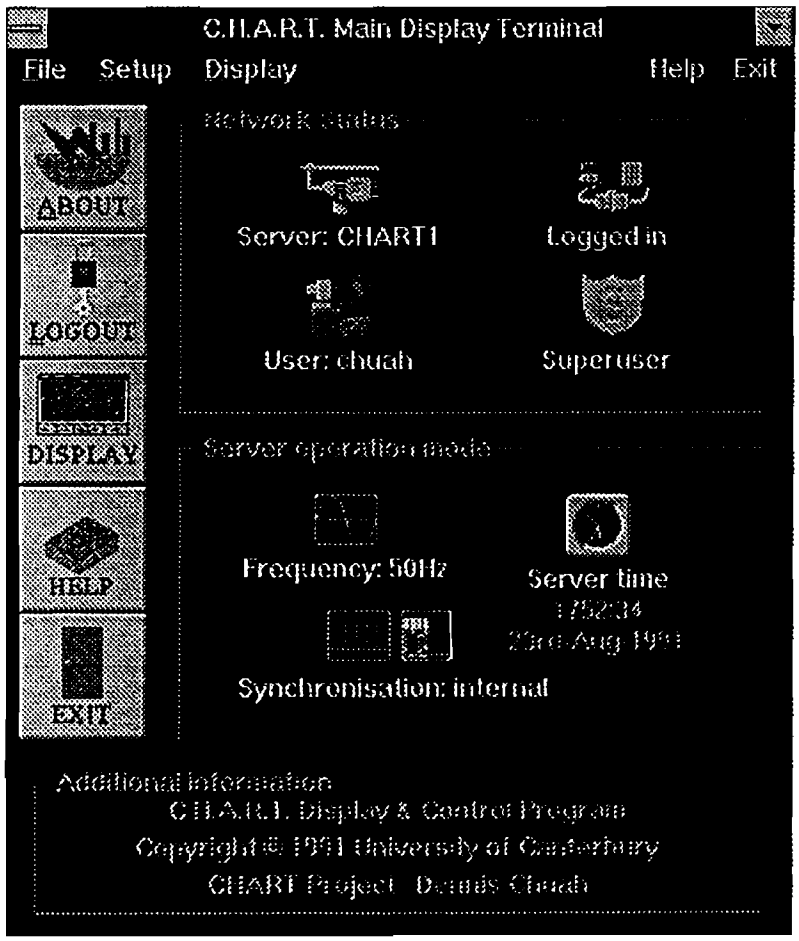


Figure 5.13 The main display terminal on the control and display workstation.

5.3 Conclusion

A very advanced data acquisition and parallel processing system aimed specifically at continuous real-time power system signal monitoring has been described. The need for the system arose initially from the desire of Transpower N.Z. Ltd., who supported the project, to accurately monitor the presence of power system harmonics on the New Zealand national grid [Goodwin, 1986]. The system described in this chapter is the latest version to evolve from the research activities over the last 6 years of the Power Systems Group at the University of Canterbury into power harmonic measurement. It is significantly different from the earlier version introduced in Chapter 3 and provides a precision time referenced measurement capability which has hitherto not been possible. No other systems are known to the author which have the capability of continuous harmonic monitoring and analysis, with the ability to precisely time stamp data.

The key features of the system which distinguish it from other data acquisition systems (usually PC based) or instruments which are capable of measuring harmonics are embodied in the system acronym CHART. Continuous measurement indicates that there is no break in the acquisition and processing of source data thus ensuring the integrity of the measured signals. Real-time capability provides the facility to observe the processed results as they occur. The on-line analysis of the processed data effectively enables efficient monitoring, analysis and storage of power system harmonic information - experience has shown that dealing with the large quantity of data collected in itself can be a major impediment to properly policing harmonic pollution. The multi-channel modular nature of the system means that it can be tailored to a wide range of power system monitoring configurations. Furthermore the Ethernet network facility enables it to be readily integrated into existing SCADA system controllers and to be accessed by any number of workstations. Another key feature of the system is the remote analog to digital data conversion at the transducer end with a digital fibre optic interface which minimizes noise and earth loop problems while ensuring maximum signal bandwidth, resolution and integrity. Finally the incorporation of a highly accurate widely accessible time reference by the use of the GPS satellite signals provides the system with the unique capability of being able to time stamp acquired data to within 1 microsecond. This last feature, by employing multiple independent systems, will provide simultaneous power measurements across a complete transmission power grid with a timing precision that has not been possible before.

The design details described in this chapter identify the important technical considerations in providing the performance and flexibility sought in such a monitoring system. The choice of bus architecture, bus bandwidth, true multi-processing capability and the real-time multitasking operating system are key elements in the design of a flexible and powerful parallel processor measurement system. The inherent flexibility of the system with its time stamping facility also enable the application to be extended to transient measurements which find ready application in, for example, HVdc fault location. The system has been tested in the laboratory environment and was used in the commissioning tests for the upgraded New Zealand inter island HVdc link in October and November, 1992. These tests are documented in Chapter 7.

Owing to delays in the production of TCP/IP for iRMX/Multibus II systems, it has not been

possible to commission the Ethernet link between the PC workstations and the 486/133SE Multibus II computer. As a 'stop-gap' solution, a spare serial port on the 486/133SE has been used to mimic this link, with an obvious reduction in the rate of data exchange between the computers.

The major part of the design details presented in this chapter have been gathered to form a paper presented at the 1992 IEEE Power Engineering Society Winter Power Meeting in New York. The paper was very well received at the meeting, and as a result of its presentation, has been published in the Transactions of the Power Engineering Society, indicating the international interest in such a monitoring system [Miller and Dewe, 1992c].

Appendix 5A Multibus II and iRMX

With huge advances in silicon technology in the 1980's, large systems were integrated into single board subsystems. An example of a single board subsystem is the 486/133SE single board computer used in the CHART project. This consists of a 33MHz 80486 CPU, a math coprocessor, 16MByte of RAM, serial ports, a parallel port, a SCSI interface, a Multibus II central services module, a full Multibus II interface, and an Ethernet connection, all on a single printed circuit board that fills only one slot in a 19 inch rack. Previously, in the CHART I system, five cards would have been required to perform all of the functions performed by the 486/133SE computer. This level of integration has had a large impact upon systems architecture, with multiples of these subsystems being used to build systems with tremendous capabilities. As a consequence the backplane bus has had to take on the additional role of a subsystem-to-subsystem communication channel. This type of system can be viewed as a Local Area Network (LAN) where a solution is functionally partitioned - separate subsystems are used to solve different facets of an overall problem.

The CHART II parallel processing system discussed in Section 5.2.2, and illustrated in Figure 5.14, is an example of this. Each of the cards in the system are independent from the others, and have been optimized for their individual tasks in isolation with respect to other cards in the system. The DAPM subsystems, for instance, are essentially single printed circuit board, single slot, processor cards consisting of dual channel serial digital fibre optical interfaces to remote ADCs for data acquisition, dual digital signal processors for processing the acquired data, an 80186 microcomputer for monitoring the processed data and for an intelligent interface to Multibus II, a serial port, and a full Multibus II interface. The DAPMs comprise specially configured hardware and software tuned for the task of analysis of power system voltage and current signals. The system is scalable to larger systems by simply adding more DAPMs - as the processing needs grow (as the number of channels increase) more real-time application boards can be easily added to increase the systems potential. Moreover, each of the subsystems in this system are individually upgradeable, allowing new technology to be applied at various points in the system without a major overhaul of the complete system. The subsystems are also independent, capable of completing their assigned tasks in isolation and need not be connected to the backplane LAN to function. They are connected to the LAN to enable the sharing of data.

The software model for this functionally partitioned solution is 'protocol based' with 'data movement'. In this type of model the computer population is split into server systems and consumer systems. A server system provides facilities and resources to the network such as file systems, or access to a communications hierarchy. A consumer system does work using the facilities provided by the network servers. In the CHART system, the DAPM subsystems are treated as compute and data servers, and the 486/133SE subsystem as a consumer system, as well as a file and communication server. The 486/133SE consumer makes defined requests for data to the DAPMs that they respond to, as illustrated in Figure 5.15.

In the loosely coupled architecture defined by Multibus II, communication is via an address space called message space - boards do not share code or data memory space. Consequently data

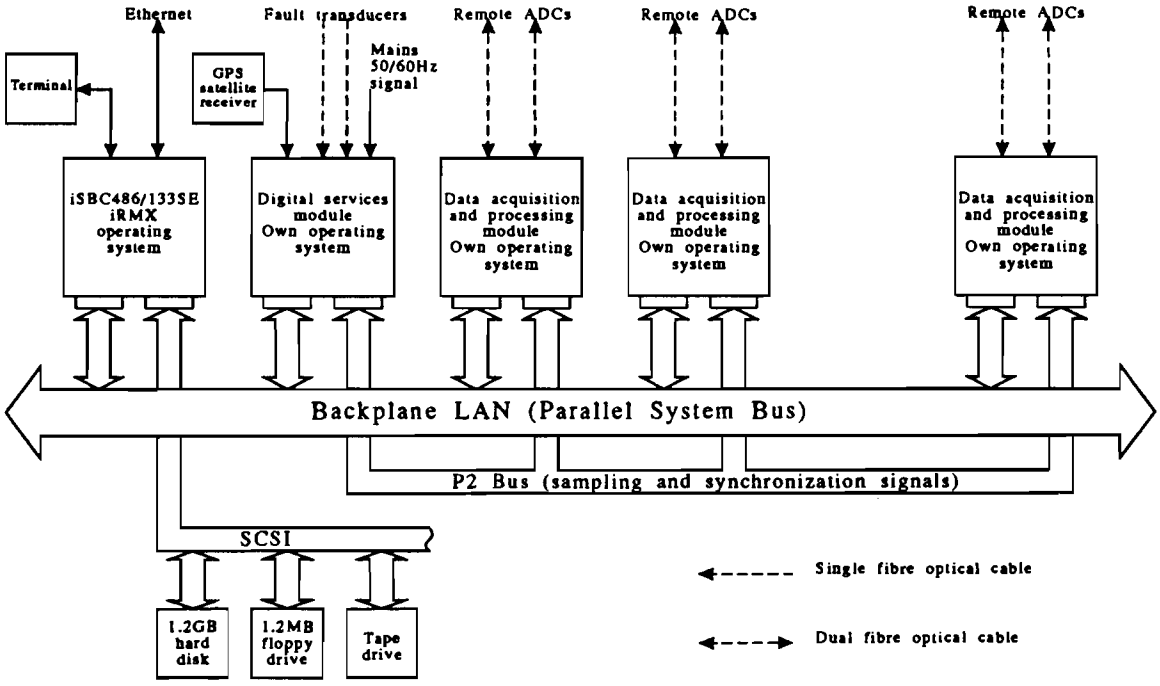


Figure 5.14 The CHART II parallel processing system.

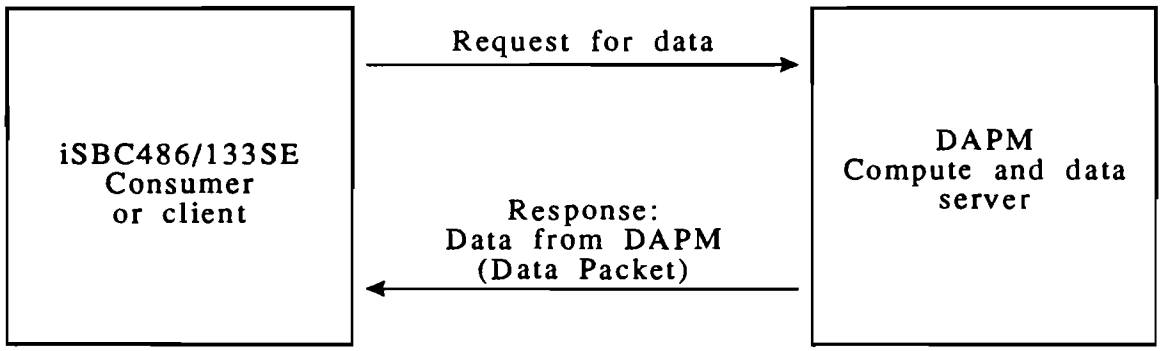


Figure 5.15 Illustration of a request response transaction in a client server system.

transfers are not processor or operating system dependent and communication among a variety of processors and operating systems can be supported in a single system chasis. In the case of CHART, the 486/133SE computer runs Intel's RMX real-time operating system because it must respond in real-time to the DAPMs and to remote users, while the DAPMs run a streamlined operating system written by the author, which adheres to the Multibus II message passing protocol.

This appendix gives an overview of the Multibus II Systems Architecture (MSA) which is used as the bus architecture in the CHART system, and discusses some aspects of Multibus II and iRMX relevant to the CHART project.

(1) Multibus II Systems Architecture

The networked-subsystems structure described above has been used by Intel to define the Multibus II systems architecture. MSA includes hardware, firmware, and software, with its base being

a disciplined backplane bus on which layers are built. The Multibus II bus specification is standardized as IEEE/ANSI 1296. It is a parity protected 32 bit synchronous bus design using a 10MHz system clock that can reliably drive a 21 slot TTL backplane.

The predecessor of Multibus II, Multibus I, used hardwired interrupt lines, which were inadequate for standardized inter-subsystem communications. Multibus II introduced a hardware-recognized data type, called a packet, which is the fundamental unit of information interchange between intelligent bus interface devices, enabling packet based signaling instead of electrical interrupt signals hardwired on the bus.

The Multibus II bus standard defines four address spaces within its physical layer. Two of these are typical of traditional back plane bus functions - off board memory and I/O accesses. Two additional address spaces realize the new requirement of a subsystem communication channel - interconnect space (for system initialization) and message space (for the run time environment).

MSA is designed to reduce the amount of work required to bring a system solution to market. All of the fundamental architecture work for initializing, diagnosing, booting and operating a multiple hetergeneous microprocessor system has been standardized and is available. Ideally this allows users to focus on the application rather than low-level implementation details.

During the system initialization phase of an MSA system, individual subsystems that may contain different architecture microprocessors and will probably be running different software are brought into an operational state. MSA details individual board tests, subsystem communications testing, system level diagnostics and a comprehensive boot protocol.

Figure 5.16 shows the stages that two typical subsystems pass through during initialization. Subsystem A has a local peripheral (SCSI) from which it boots, while subsystem B has no locally attached device and boots dependently via subsystem A.

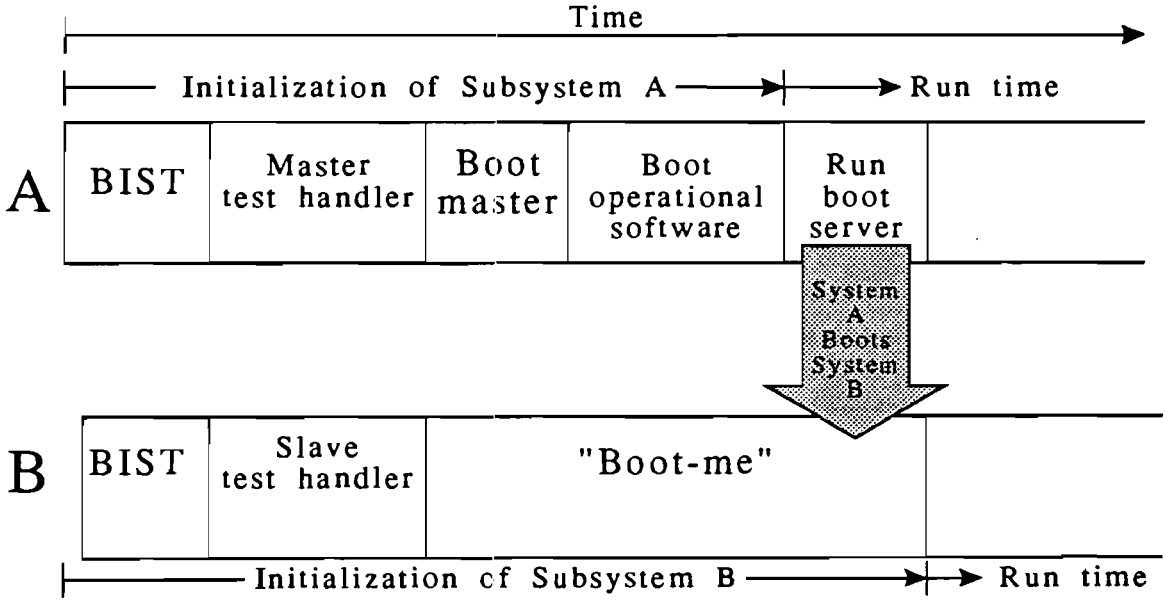


Figure 5.16 The MSA initialization and run time phases.

In the run time environment, software layers built on the MPC hardware device handle

connections between nodes in the system and data buffer fragmentation on transmission and reception of messages. These software layers have been implemented on different operating systems (UNIX and iRMX for instance), allowing subsystems to run these and support Multibus II at the same time. As mentioned previously, a special operating system has been written for the DAPMs designed for the CHART project, and this operating system implements in full the MSA run time software layers.

(2) Multibus II Message Passing Concepts

The fundamental unit of information interchange between Multibus II computers is the hardware recognized data type called the packet. A packet consists of 32 bytes of data, 8 of which are the header (giving packet type, source address, and destination address), with the remaining 24 bytes used for data. The exchange of a packet from one Multibus II computer (an agent) to another is referred to as an *unsolicited message*. Transfers of large amounts of data between agents are referred to as *solicited messages*, because the transfer is solicited by smaller unsolicited messages. Solicited message transfers in the CHART system follow the client server model, where an *RSVP* request from the client to the server for data is made by an unsolicited message. In the example given by CHART, the 486/133SE requests data from DAPMs. On receipt of a request, if a DAPM has data, it requests a buffer from the 486/133SE (using a *buffer request* unsolicited message) and waits for a return *buffer grant* unsolicited message. This message automatically begins a transfer of data between the two agents, which usually uses DMA devices on each agent.

Messages are addressed by a *socket*, which is a combination of an agents slot number and a *port* on the agent. CHART utilizes this addressing scheme to produce an array of unique addresses over Multibus II for each DAPM. The operating system running on each DAPM is identical, as is the DAPM hardware. The port addresses on each DAPM for certain functions, such as executable down loading or harmonic data collection, are also the same, but when combined with the slot number to form a socket address, they become unique addresses. Hence the 486/133SE computer can uniquely address any DAPM port in the system. A *broadcast* message can be sent to a port on all DAPMs simultaneously, as opposed to an ordinary unsolicited message that is addressed to a port at a certain slot.

(3) Multibus II Interconnect Space

The Multibus II interconnect space arose out of a need to reduce the complexity of advanced computer boards. This was achieved by replacing jumper options to select such things as interrupt routing, memory mapping, EPROM size, and the use of other installed components with firmware configurations options. Interconnect address space is defined in the Multibus II IEEE 1296 specification. It solves three major problems: board identification, configuration, and diagnostics. Interconnect space is almost always implemented on a Multibus II computer using the Intel 8751 microcontroller in conjunction with the MPC device. In essence it consists of a set of 512 registers used for board identification, configuration, and diagnostics, that can be accessed by any other computer on the Multibus II backplane.

The board identification registers are read-only locations containing board information such as type, manufacturer, components installed, and other board specific functions. The configuration registers are read/write registers which allow the system software to set and change the configuration of many on-board hardware options. This enables hard-wired jumper options to be eliminated in favour of software control. The diagnostic registers are used for the starting, stopping, and status reporting of self contained diagnostic routines supplied with each computer (commonly known as Built In Self Tests (BISTs).

The CHART II instrument uses interconnect space to identify DAPMs during the initialization of the system. This is performed by the centralized 486/133SE scanning the backplane using the board identification registers of interconnect space and geographically locating DAPMs within the backplane using 'cardslot' numbering. From this the operating system running on the 486/133SE computer generates a map of where DAPMs are located, which is used as a base address list for message passing. This has the tremendous advantage of allowing new DAPMs to be added to the system without the need to reconfigure system software - an extra DAPM is automatically recognized during system initialization, and is configured into the operating system running on the 486/133SE. All computers in the system carry their own initialization and diagnostic functions on-board in firmware, which achieves cardslot independence.

(4) Intel's Real-Time Multitasking Operating System - iRMX386

The iRMX386 operating system is designed for use with Intel's single board computers built around the 386 and 486 microprocessors. It offers a broad range of functions including:

- Monitoring and controlling unrelated events occuring outside the SBC.
- Communication with a wide variety of I/O and mass storage devices.
- Message passing and interconnect space support for Multibus II.
- A base on which to run a number of languages and other software tools.

In the CHART II system, the 486/133SE computer runs the iRMX386 operating system. The real-time response and multitasking ability of the operating system is utilized to collect data from DAPMs and to send data to display workstations. One task per DAPM is created (from the table of DAPMs identified during initialization using interconnect space) which collects data using the client server model discussed previously, and stores it to a mass storage device. Data is also passed to a task that sends data to display workstations. The iRMX operating system allocates CPU time by a *preemptive priority-based* scheduler. In this system, any time that a task has a higher priority than the currently running task, a task switch is made and the higher priority task begins to run. A variation on time-sliced scheduling called *round-robin scheduling* can be used by iRMX to cause tasks of equal priority to take turns at running.

Access to Multibus II transport protocol by iRMX is provided by *ports*. Ports are access points to the bus through which messages can be sent or received. *Buffer Pools* can be attached to ports to facilitate buffering of data received at a port. A buffer pool is esentially a pool of memory

allocated during task setup for receiving messages. Having this pool of already allocated memory available cuts down on system overhead because creating and deleting segments of memory is slow. A *short circuit message* is an exchange between ports on the same processor card using Multibus II message passing, and can be used for intertask communication. The MPC device is bypassed in this case.

Mailboxes are used for intertask communication. One task can send a token for data to an already created mailbox, while another task can request the token from the mail box. If the token isn't at the mailbox, the requesting task can wait indefinitely, for a certain length of time, or not wait at all.

Software for the DAPMs[7] and the DSM is developed on the 486/133SE computer under iRMX386 using supplied software development tools and the hard disk drive. All 486/133SE software is also developed on the 486/133SE under iRMX386.

Appendix 5B Sample Rate Multiplier Accuracy

This appendix gives the derivation of SRM accuracy given by Equation 5.1 of Section 5.2.2.3(a). Accuracy is based on how finely the spacing of the output samples can be adjusted to match one fundamental period by changing the SRM counters initial count by one. It is assumed that the fundamental frequency changes slowly enough to allow the SRM to track it.

The change in equivalent fundamental frequency at the SRM output caused by the initial count on the SRM counter changing by 1 is given by

$$\begin{aligned}\Delta f &= f_1 - f_2 \\ &= \frac{f_{clk}}{1024 count_1} - \frac{f_{clk}}{1024 count_2} \\ &= \frac{f_{clk}}{1024}\left(\frac{1}{count_1} - \frac{1}{count_2}\right) \text{ Hz.}\end{aligned} \tag{5.3}$$

Where $count_n$ = 0FFFFh - (the counters initial count), and f_{clk} is the SRM clock frequency. Now $count_1 - count_2 = 1$, and $count_1 \simeq count_2$. Therefore

$$\Delta f \simeq \frac{f_{clk}}{1024}\left(\frac{1}{{count_1}^2}\right) \text{ Hz,} \tag{5.4}$$

and since $count_1 = \frac{f_{clk}}{50\text{Hz} \times 1024}$ when there are exactly 1024 samples per cycle,

$$\Delta f \simeq \frac{1024(50)^2}{f_{clk}} \text{ Hz.} \tag{5.5}$$

Which is the approximate SRM accuracy.

[7]This is the 80186 software development only. DSP software is developed on a PC.

Appendix 5C CHART System Components

This appendix shows a number of photographs of components in the CHART system.

Figure 5.17 Remote Data Conversion Modules (RDCMs) in the Benmore 220kV switch yard.

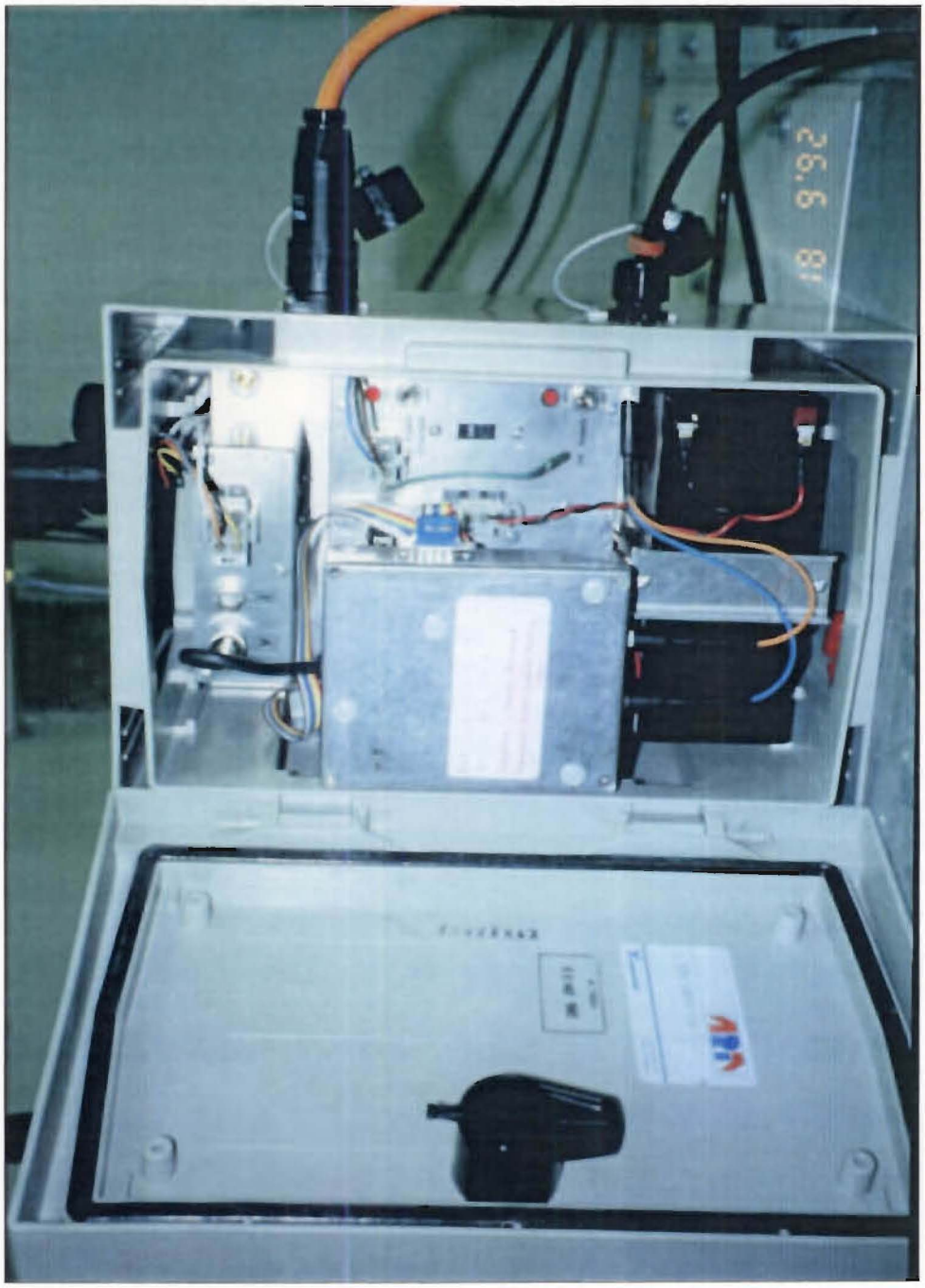


Figure 5.18 Remote Data Conversion Module (RDCM).

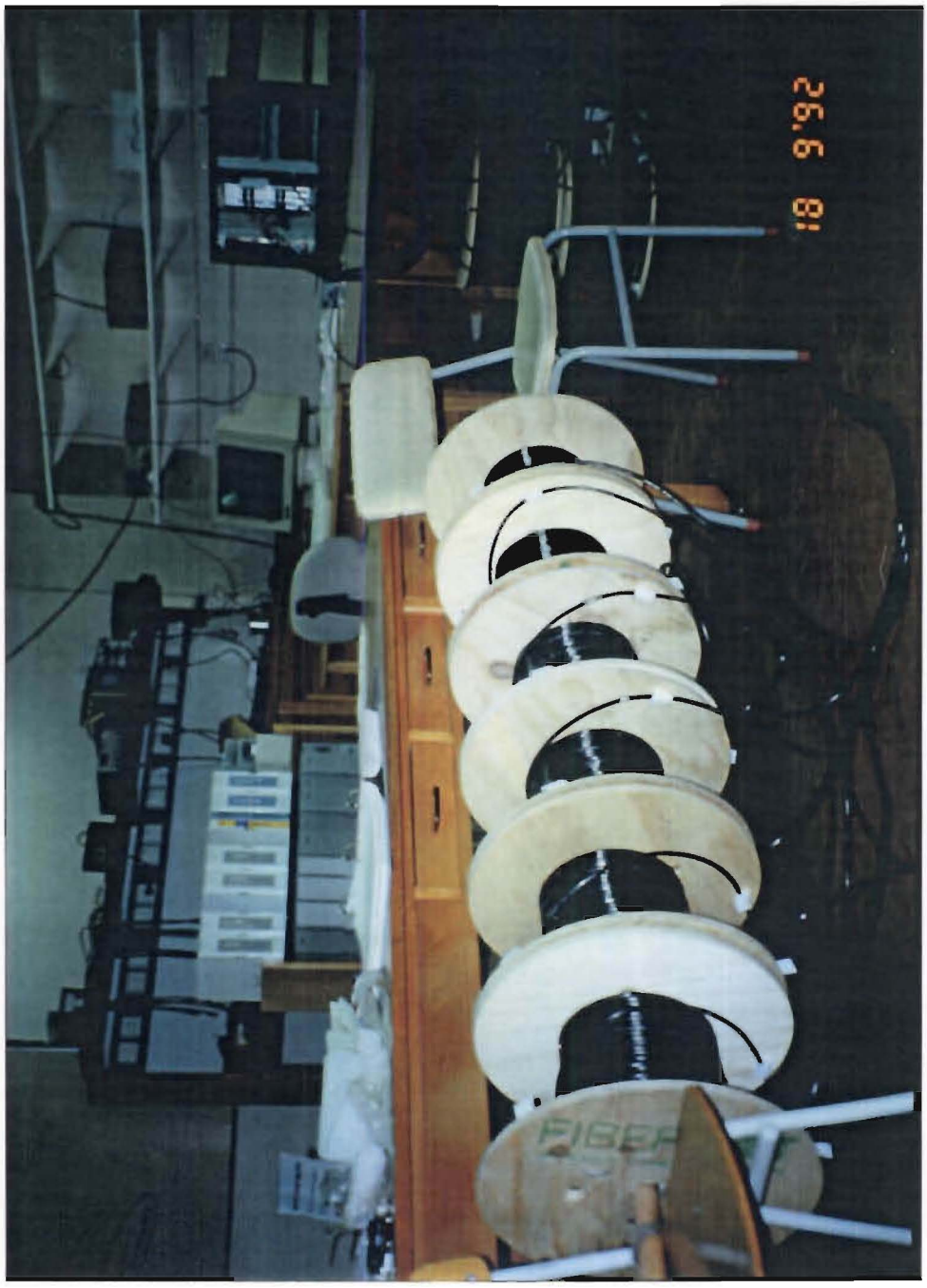


Figure 5.19 Fibre optical cable drums.

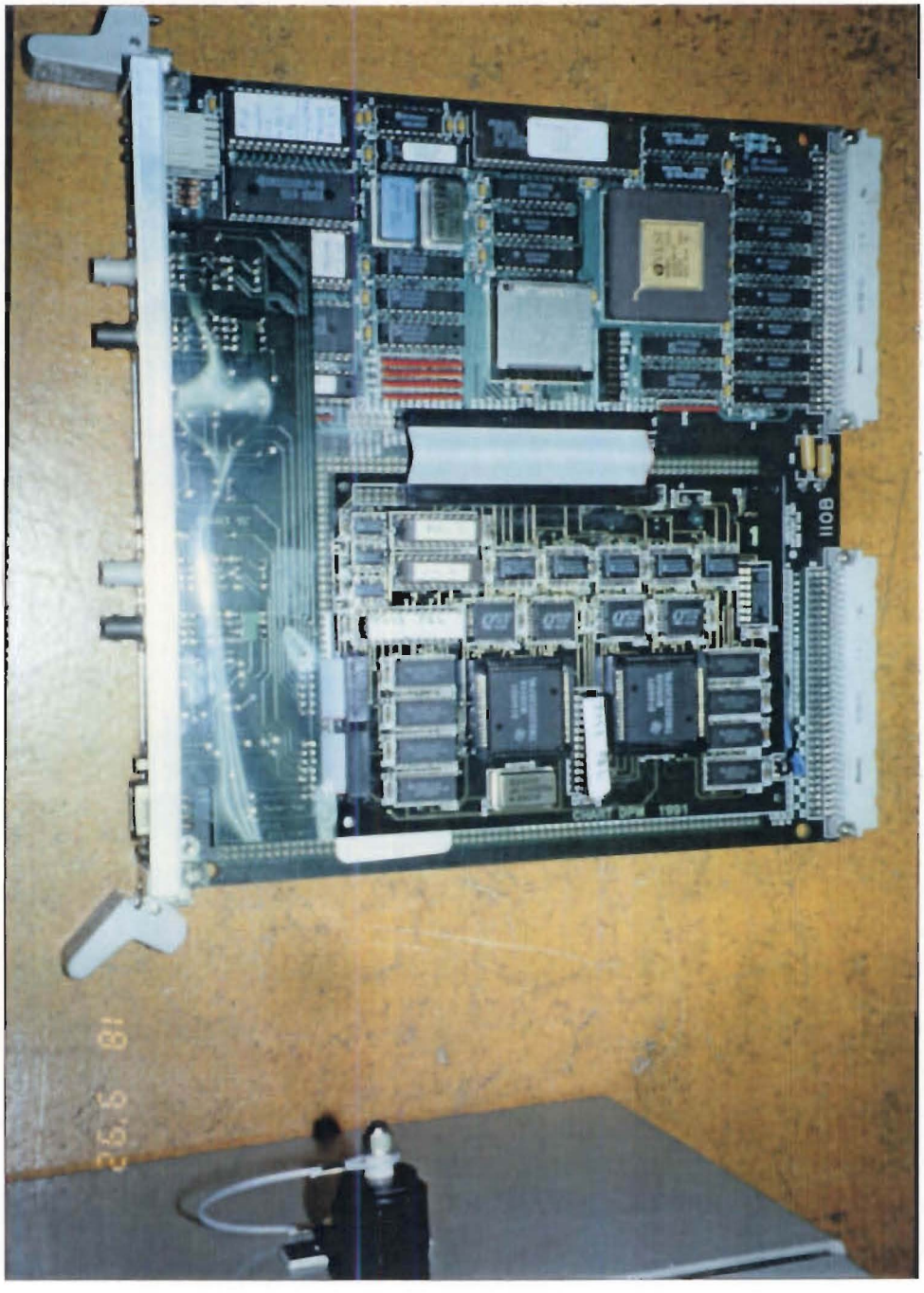


Figure 5.20 Data Acquisition and Processing Module (DAPM).

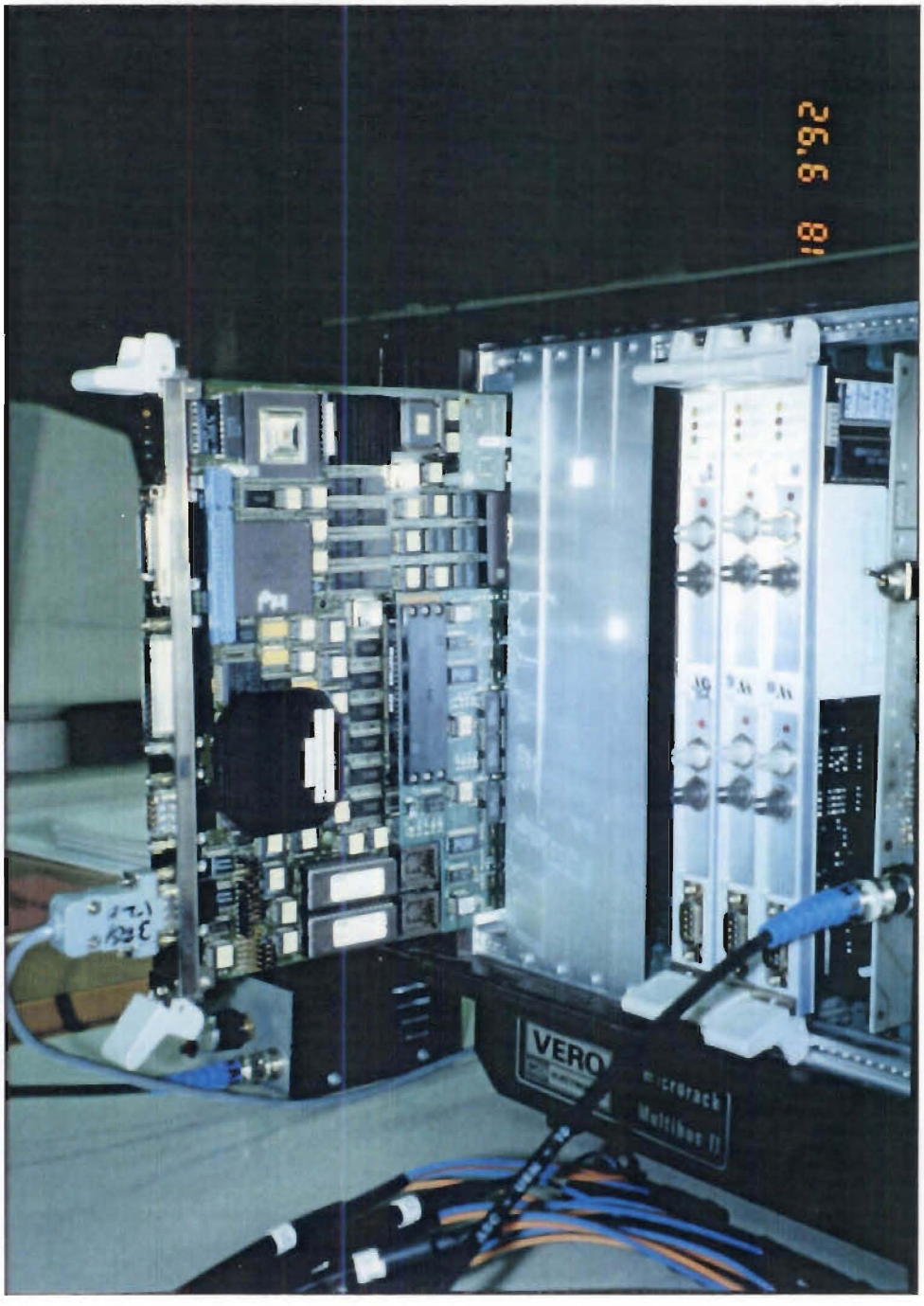


Figure 5.21 Multibus II 486/133SE computer.

Figure 5.22 The CHART Parallel Processing Unit (PPU) and display PC.

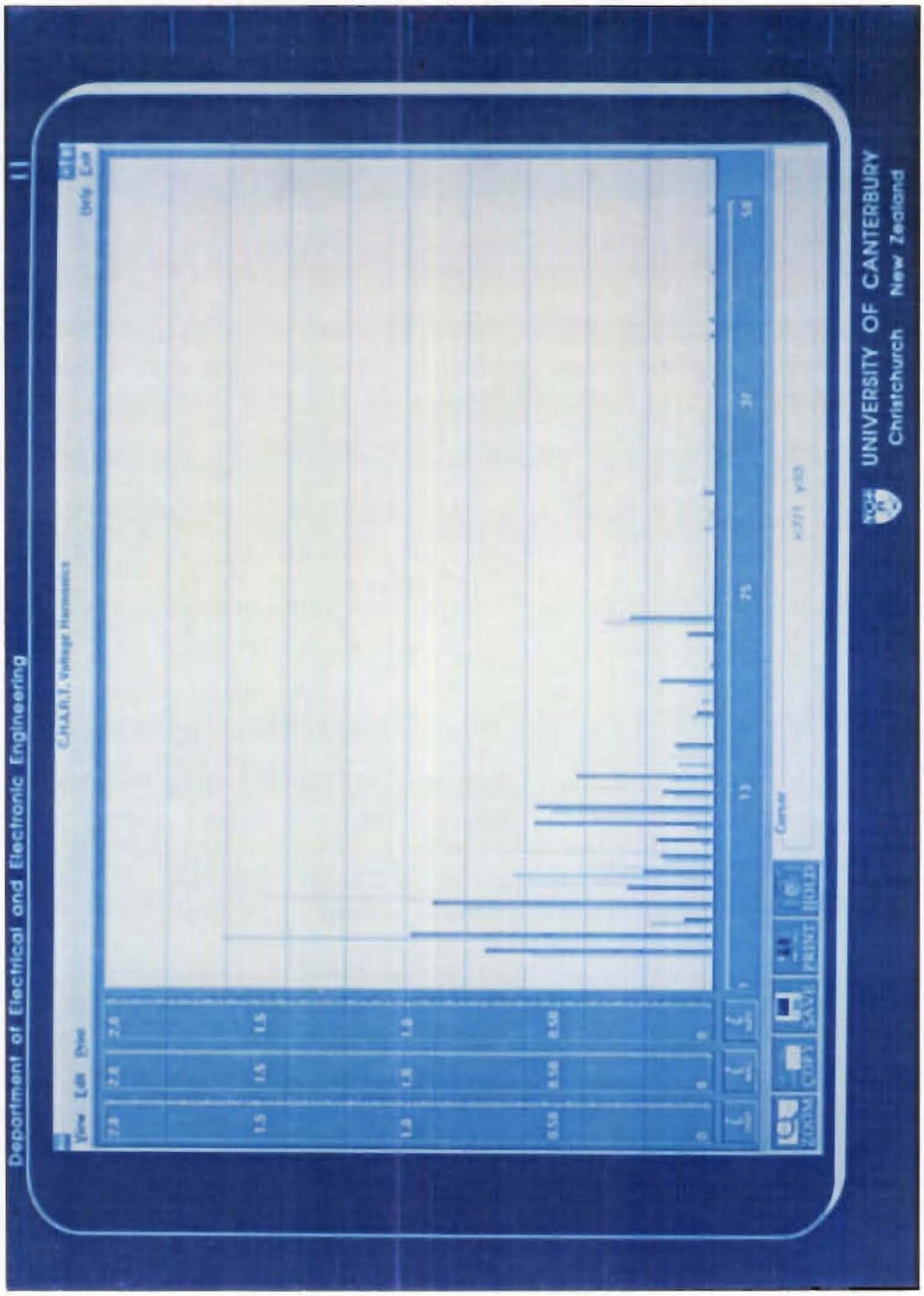


Figure 5.23 A typical display of harmonic data.

Chapter 6

DIGITAL SIGNAL PROCESSING TECHNIQUES USED IN HARMONIC ANALYSIS

6.1 Introduction

Digital signal processors are used extensively in CHART II to implement the processing algorithms required to filter and transform time domain signals to harmonic levels. This chapter establishes concepts important to digital harmonic analysis, and describes the digital signal processing techniques used in the CHART project to compute voltage and current harmonic levels.

The DFT is used by CHART to find spectral information about voltage and current signals. This is computed by DSPs using an FFT algorithm, which requires the continuous time varying voltage and current signals to be represented by a set of digital samples of discrete magnitudes, taken at discrete instants in time. This sampling process can cause aliasing in the sampled signal, and quantization to discrete levels introduces a quantization noise. Aliasing and quantization are introduced in the first section where it is shown how to avoid noticeable aliasing. This section also introduces sampling concepts important to later sections.

Analysis of a signal using an FFT also requires a finite set of samples. This means that the signal being sampled must be truncated, which may distort the spectrum produced by the FFT, essentially causing the interference of one harmonic with another (known as spectral leakage). The extent of this interference is discussed and it is shown how CHART minimizes it by sampling coherently with the periodic fundamental frequency. The finite set of samples taken by CHART for FFT analysis corresponds to exactly one cycle of the fundamental. FFT analysis is therefore performed on a cycle-by-cycle basis, producing a set of harmonics for each cycle. In order to reduce interference from non-harmonic signals that may be present in an acquired signal, as well as reducing the data rate for the FFT, consecutive cycles of a voltage or current waveform can be averaged to one. The principle of averaging is discussed and it is shown how it can be used to reduce processing requirements while preserving the FFT bandwidth for harmonic analysis.

After establishing the principles of anti-aliasing filtering, sampling for the FFT, and averaging, this chapter goes on to describe a multirate DSP technique for determining voltage and current harmonics using the CHART II instrument. The technique utilizes a polyphase decimation finite impulse response (FIR) filter as an anti-aliasing filter, followed by a real valued FFT algorithm to find harmonic levels (both magnitude and phase). The design of the FIR filter is discussed, covering both the coefficient determination and its structural manipulation for computational efficiency. The

use of a digital anti-aliasing filter simplifies the analog anti-aliasing filter preceding the ADC. This is important in the CHART II instrument, as the data acquisition modules are located at remote sites, and must have a low power consumption as well as being physically small.

Finally the implementation of the 128-point FFT is discussed and the data flow through the system and scheduling of the FIR filter and FFT tasks on the DSPs is summarized. The results of timing tests on these algorithms are presented, and it is shown that the CHART instrument can execute them together in real-time.

6.2 Data Acquisition

The approach adopted in the determination of voltage and current harmonic levels using the CHART instrument is one of digital signal processing. In this approach the DFT

$$H(\frac{n}{NT}) = \sum_{k=0}^{N-1} h(kT)e^{\frac{-j2\pi nk}{N}}, \text{ for } n = 0, 1, \cdots, N-1 \tag{6.1}$$

is applied over an integer number of fundamental cycles using an FFT algorithm, where N is the number of samples taken and T is the interval between samples. This is an approximation to the continuous Fourier transform, transforming the samples of the repetitive signal $h(kT)$ to the frequency domain, $H(\frac{n}{NT})$.

The application of the DFT requires that voltage and current waveforms be represented by a set of digital samples of discrete magnitudes, taken at discrete instants in time. The *sampling* process is accomplished by multiplying the voltage or current waveform, represented by $h(t)$ in figure 6.1(a), by the sampling function $\delta_0(t)$, illustrated in figure 6.1(b). This results in a signal

$$\hat{h}(t) = \sum_{k=-\infty}^{\infty} h(kT)\delta(t - kT) \tag{6.2}$$

which is a set of uniformly spaced samples, T seconds apart, illustrated in figure 6.1(c). The sampling period is defined as T and the sampling rate as

$$f_s = \frac{1}{T}. \tag{6.3}$$

For a unique correspondence between the continuous function $h(t)$ and its samples $\hat{h}(t)$, the sampling period T must be chosen to satisfy the requirements of the Nyquist sampling theorem [Linden, 1959] which essentially states that the signal $h(t)$ must be band-limited to f_a and that

$$f_s > 2f_a. \tag{6.4}$$

This is illustrated in figure 6.1(c) which depicts the Fourier transform of the sampled signal. If this condition is not met, the spectrum centred at f_s will overlap with that at 0, distorting the sampled signal - an effect known as *aliasing*.

In practice it is impossible to completely band-limit a signal, a problem circumvented by low pass filtering the signal before sampling, and sampling at such a rate that aliasing is negligible.

The level below which aliasing is negligible is the signal noise floor, determined predominantly by quantization noise, discussed in the following section.

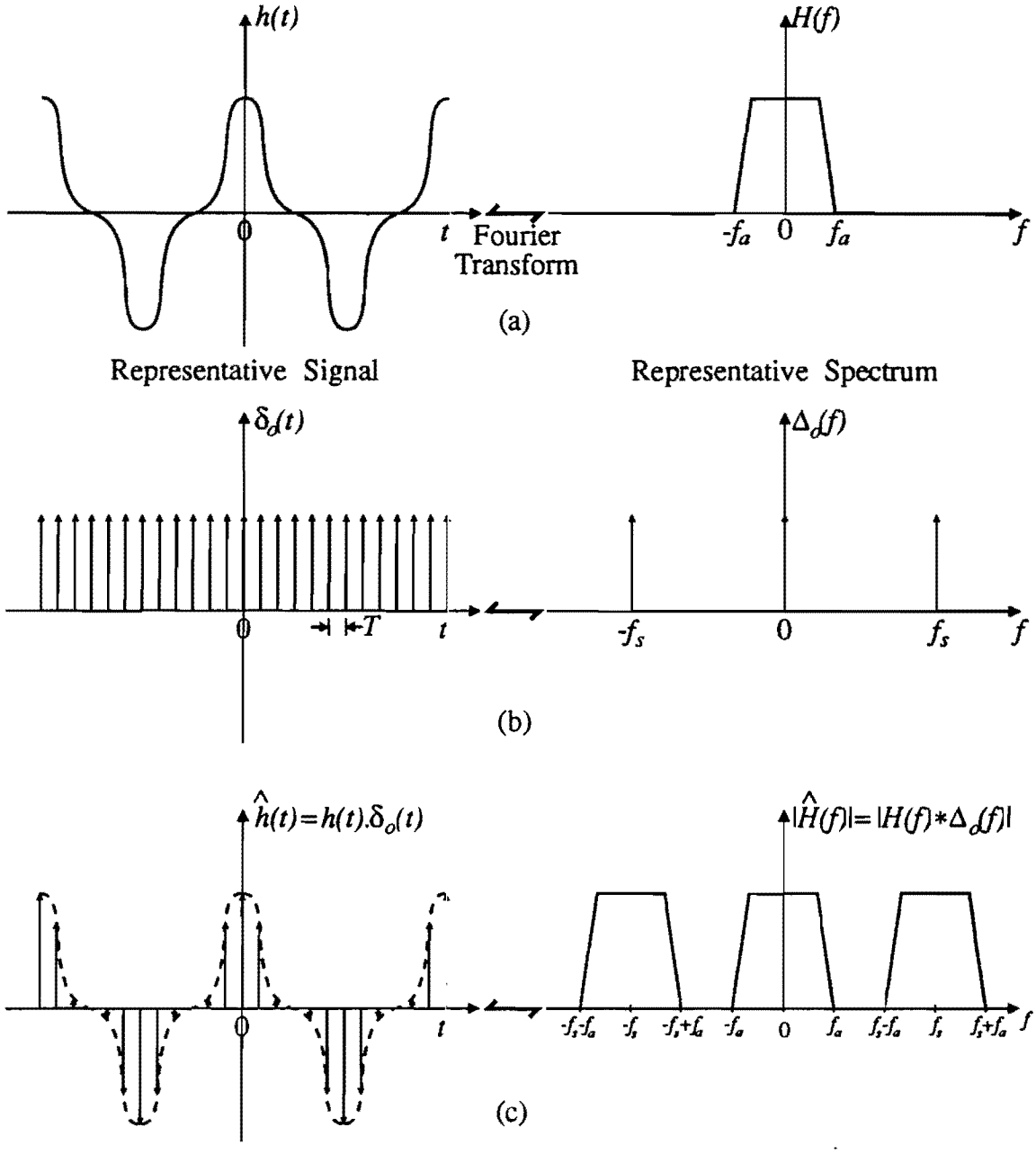


Figure 6.1 Sampling of a signal.

6.2.1 Signal Quantization

The sampled signal must be quantized to a number of discrete magnitudes for it to be represented by a finite word length machine. Quantization is usually performed during analog to digital conversion, and creates a quantization noise voltage. The approximate theoretical RMS signal to quantization noise ratio of an N-bit ADC for a full scale sinewave input is given by [Bennett, 1948]

$$SNR(dB) = 6.02N + 1.76. \tag{6.5}$$

This provides a noise level below which aliasing is negligible, as the aliased signal will not be resolved by the convertor, giving an indication of the filter response required to avoid noticeable aliasing.

This filter response is depicted in figure 6.2, with the aliased response shown dotted about f_s. The filter has a roll-off from the cut-off frequency f_c to f_a which is sufficiently steep to ensure an attenuation of A dB at f_a when $f_s = 2f_a$. This assumes that the signal being sampled may contain frequency components of full power beyond the cut-off frequency. Such a stringent filter may not be required for real signals.

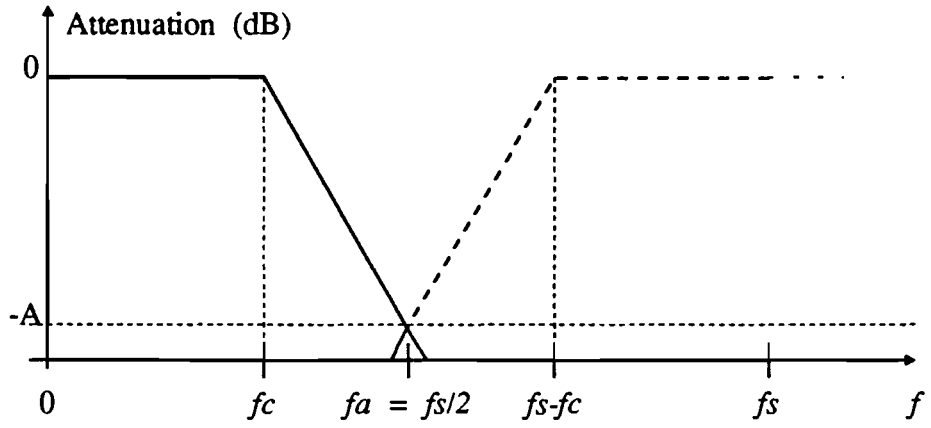


Figure 6.2 Anti-aliasing filter response.

It is an approximation to apply equation 6.5 to the signals measured on a power system which may be distorted from an ideal sinewave. It does however give a pessimistic indication of the attenuation required to avoid aliasing and this equation has been used in this application.

6.2.2 Sampling for the FFT

The sampled signal $\hat{h}(t)$ of equation 6.2 must be truncated to a finite number of samples for machine computation. This is achieved by multiplying the sampled signal illustrated in Figure 6.3(a) by the rectangular truncation function of Figure 6.3(b) to yield the finite sequence of N samples illustrated in Figure 6.3(c). A sinewave is used to illustrate this process in both the time and frequency domains.

The Fourier transform of the rectangular truncation function is the $sinf/f$ function, also illustrated in figure 6.3(b). The Fourier transform of the sampled truncated signal of figure 6.3(c) is obtained by convolving the sampled signal's Fourier transform with the $sinf/f$ function of figure 6.3(b). If the periodic signal $h(t)$ is represented by a Fourier series expansion and is band limited to N harmonics, the sampled truncated signal's Fourier transform becomes

$$H'(f) = T_0 f_s \sum_{n=0}^{N} \alpha_n \frac{sin(\pi T_0[f - nf_0])}{\pi T_0[f - nf_0]}, \tag{6.6}$$

where α_n are the complex coefficients of the Fourier series, and f_0 is the fundamental frequency of the periodic signal $h(t)$. The derivation of this is given in Appendix 6A. Figure 6.4(a) depicts $H'(f)$, which is essentially the summation of $sinf/f$ functions centred on each harmonic frequency. The width of the $sinf/f$ functions is dependent on the truncation interval width of Figure 6.3(b). If the truncation interval is equal to an integer multiple of the period of $h(t)$ (that is $T_0 = n/f_0$, where n is an integer) the $sinf/f$ function centred on each harmonic will be maximum at the harmonic frequency and zero at all adjacent harmonics.

When the truncation interval is not equal to an integer multiple of the fundamental period ($T_0 f_0 \neq n$, where n is an integer), then the $sinf/f$ function at each harmonic will interfere with adjacent harmonics - an effect known as *spectral leakage* [Brigham, 1974]. The interference of an harmonic adjacent to another is given by

$$A(dB) = 20log_{10}|\frac{sin(\pi T_0 f_0)}{\pi T_0 f_0}|, \tag{6.7}$$

where f_0 is the fundamental frequency and T_0 is the truncation interval length. The derivation of this equation is given in Appendix 6B.

If a voltage or current signal is sampled at a constant frequency f_s such that the truncation interval corresponds to exactly one period of the 50 Hz or 60 Hz fundamental frequency, no interference from adjacent harmonics will occur. However, fluctuations in the fundamental frequency will effectively change the truncation interval, causing spectral leakage. The attenuation of adjacent harmonics is shown in Figure 6.4(b) for a nominal 50Hz fundamental. New Zealand legislation requires that this attenuation be greater than 40 dB [NZED, 1983]. It also states that harmonic voltage and current measurements shall be made when the system frequency is within 0.5 percent above or below the standard of 50 Hz. Evaluating the attenuation for the two limits of 49.75 Hz and 50.25 Hz gives 46 dB attenuation at each limit. Hence it is feasible to sample at a constant frequency for harmonic monitoring to comply with New Zealand legislation. Nevertheless, the CHART harmonic monitor is equipped with a device that produces a sampling signal of frequency f_s that is locked to the fundamental frequency f_0 such that $f_0 T_0$ is very close to unity, enabling CHART to monitor harmonics when the system frequency is well outside the limits set by New Zealand legislation. This means that it will comply with other legislation or standards that set fundamental frequency limits beyond those given in New Zealand legislation. Because spectral leakage is reduced by sampling coherently with the fundamental, windowing of the time domain data prior to FFT computation is not necessary. The sampling device is known as the *sample rate multiplier* and is discussed in section 5.2.2.3.

The FFT algorithm [Brigham, 1974] is used to efficiently compute the DFT of voltage and current signals, and as discussed previously, the transform is computed over exactly one cycle of the fundamental. In this way, the system works on a cycle-by-cycle basis, treating each cycle separately, and producing harmonic results for each cycle.[1] Harmonics up to the $50th$ are required, and in order to realize this, as well as to satisfy the sampling theorem, the sampling frequency must satisfy the relation

[1] A number of cycles may be averaged to produce one averaged cycle over which the FFT may be applied. Averaging is discussed in Section 6.4.

$$f_s > 2 \times 50 f_0, \tag{6.8}$$

where f_0 is the fundamental frequency. This corresponds to exactly 100 samples per cycle. The FFT algorithm requires a record length of $N = 2^\gamma$ samples, where γ is an integer [Brigham, 1974]. The lowest value of N satisfying equation 6.8 is 128, meaning that 128 point FFTs are required to resolve up to the 50^{th} harmonic, giving a required sampling frequency of $128 f_0$ and 128 samples per cycle of the fundamental.

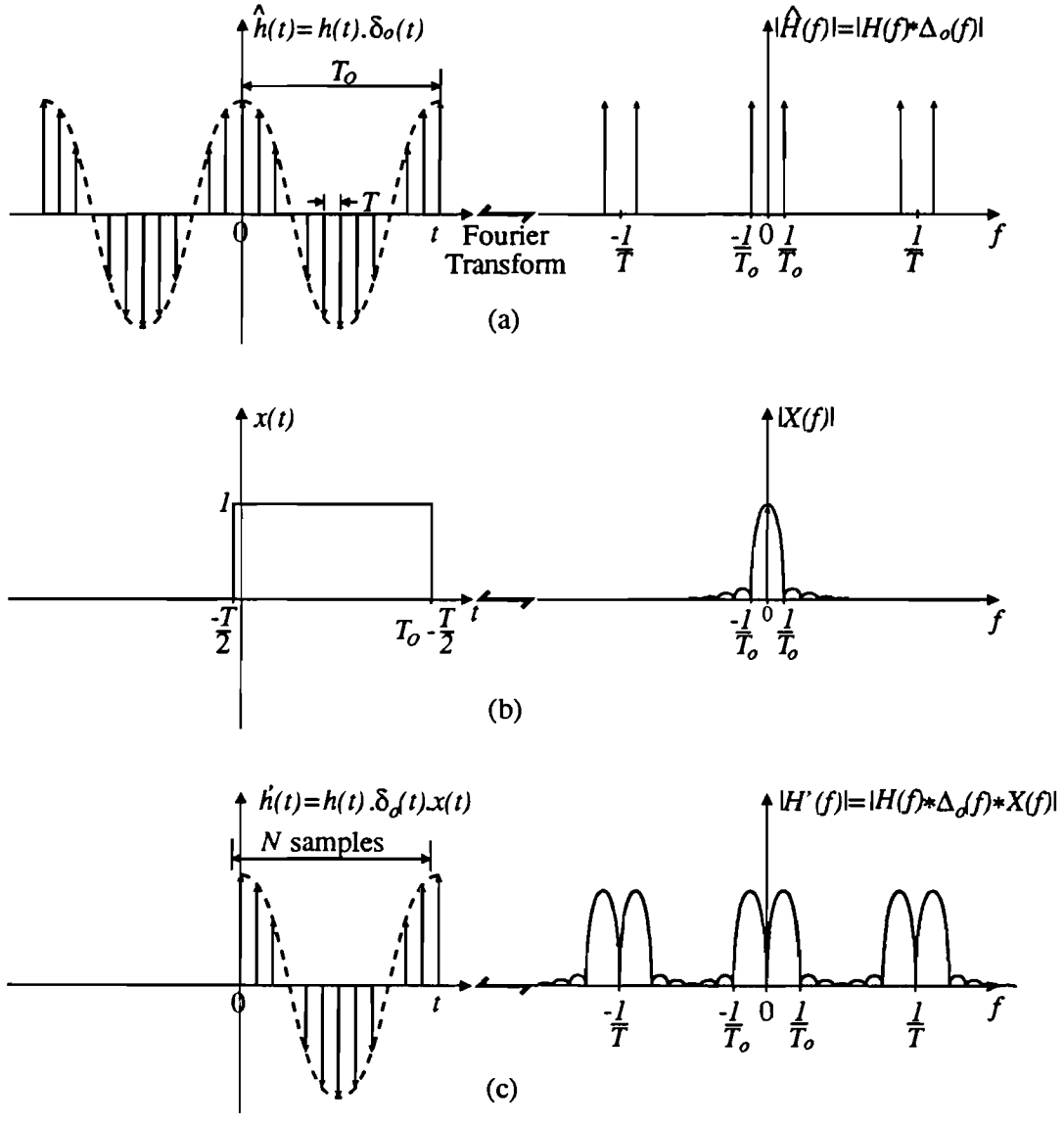
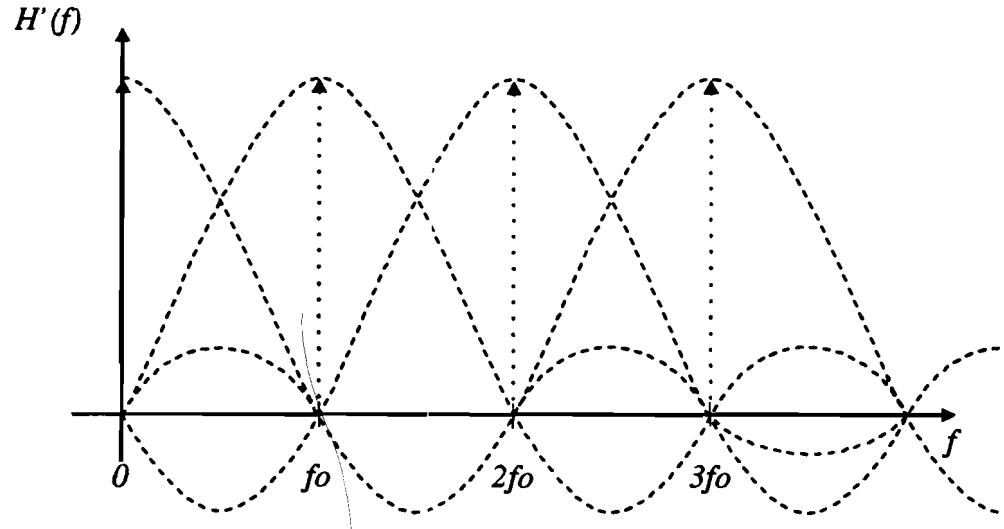
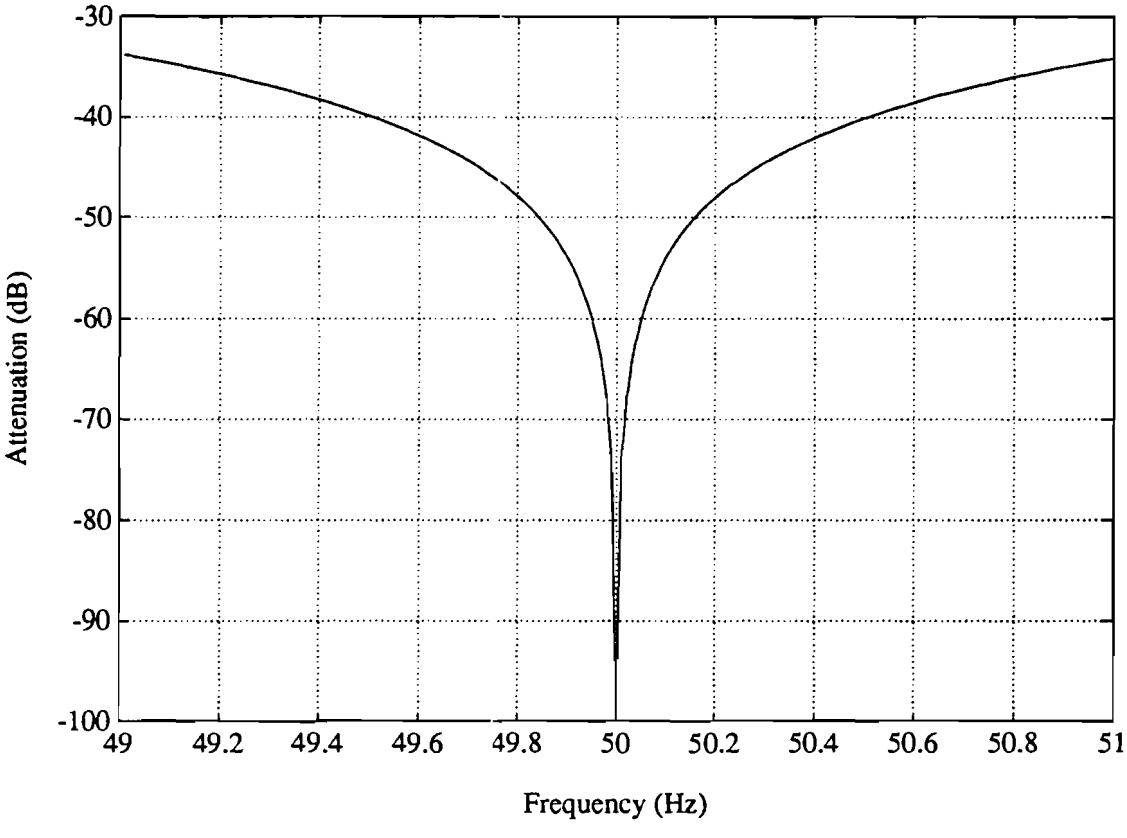


Figure 6.3 Truncation of a periodic signal and the resultant Fourier transform.



(a)



(b)

Figure 6.4 (a) The spectrum resulting from the rectangular windowing of a sampled signal. (b) The attenuation of an harmonic at an adjacent harmonic when the rectangular window is exactly equal to the period of the nominal 50 Hz system frequency, but with the system frequency changing around the nominal 50 Hz.

6.3 Anti-Aliasing Filtering

Sampling at a frequency of $128f_0$ - which is equivalent to $2.56f_{50}$, where f_{50} is the frequency of the 50^{th} harmonic - leaves a band between f_{50} and $f_s/2$ of unwanted harmonics in the FFT results, illustrated in figure 6.5(a). Because these results are not required, it does not matter if they are distorted by an anti-aliasing filter and by aliasing. Hence this band is used to implement an anti-aliasing filter with a roll-off from $f_c = f_{50}$ sufficiently steep to give 98dB attenuation at $f_s - f_c$, illustrated in figure 6.5(b). Aliasing will occur in this band, but because harmonic analysis is performed outside of it, it is of no consequence. The ADCs employed by CHART are 16 bit convertors, giving a theoretical RMS signal to quantization noise ratio of 98dB using equation 6.5.

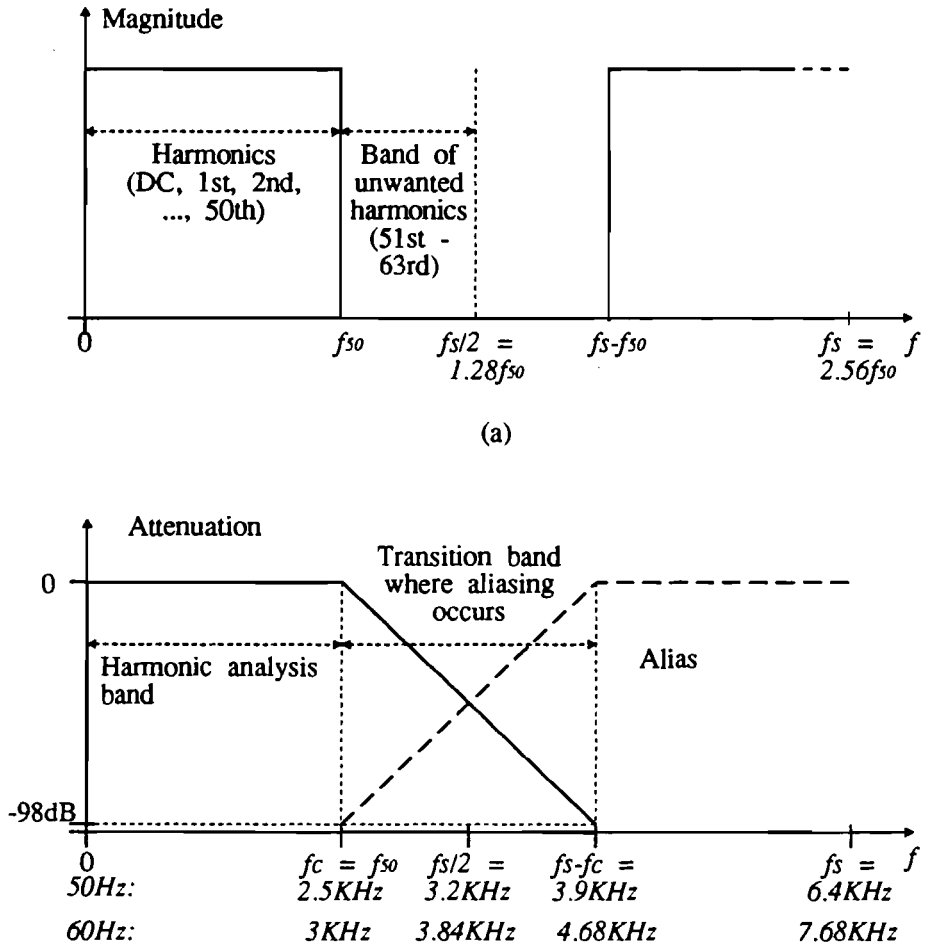


Figure 6.5 (a) Spectrum showing the band of unwanted harmonics resolved by the FFT. (b) The anti-aliasing filter response implemented inside this band.

The anti-aliasing filter required for the steep roll-off depicted in figure 6.5(b) can be realized by an analog filter, but is not practical in the CHART system which has been designed to have physically small stand-alone low power data conversion modules (discussed in section 5.2.1). The reasons for this are listed below:

- A passive analog filter requires much bulky circuitry and can be very sensitive to component variation.
- If built from active components its power consumption will be too high.
- Switched capacitor filters also consume too much power, and cause significant harmonic distortion.
- Considerable phase and magnitude distortion will occur in the vicinity of the cut-off frequency, distorting important harmonic information.
- Ideally the group delay of the anti-aliasing filter should be constant, so that all harmonics are delayed by the same amount.

The CHART instrument realizes this filter specification by using a digital FIR filter, implemented by each of its front-end DSPs. The analog voltage and current signals are sampled at a higher frequency than that required to give 128 samples per cycle. This reduces the required roll-off slope of the anti-aliasing filter preceding the ADC (illustrated in figure 6.6(b)), making its design much simpler. It can also improve the effective SNR of the sampled signal if the signal bandwidth is held constant [Crochiere and Rabiner, 1983]. This is known as *oversampling*, and is illustrated in figure 6.6(a), with the required anti-aliasing filter response preceding the convertor shown in figure 6.6(b). The CHART instrument employs an oversampling rate of $M = 8$, resulting in a sampling frequency of $1024 f_0$. This enables a simple 5 pole Butterworth filter to be used as the front end anti-aliasing filter. A 5 pole Butterworth filter was used as it has a tolerably good amplitude response and a near constant group delay in the pass-band [Zverev, 1967]. Due to its high attenuation around the the cut-off frequency, it was designed to have a cut-off slightly above the $50th$ harmonic, minimizing distortion to harmonics around the filter cut-off. An oversampling rate of 8 was settled on as a compromise between the analog filter being very simple (achieved with M large), and leaving a sufficient amount of time available for FFT computation by the DSPs (achieved with M small).

FIR filters have a number of features suited to this application. These are:

1. Linear phase.
2. Easy design and implementation.
3. They are always stable.

6.3.1 Anti-Aliasing FIR Filter Design

As discussed previously, the sampled signal $\hat{h}(t)$ must be re-sampled at a lower rate for FFT computation. Because it may contain frequency components beyond the now lower Nyquist limit when re-sampling (or down converting), it must be band-limited by an anti-aliasing filter. This is performed on the digital samples using a FIR filter. The implementation of FIR filters using DSPs is well documented [Chassaing and Horning, 1990], and the TMS320C26 DSP has an architecture and instruction set that can implement the convolution equation

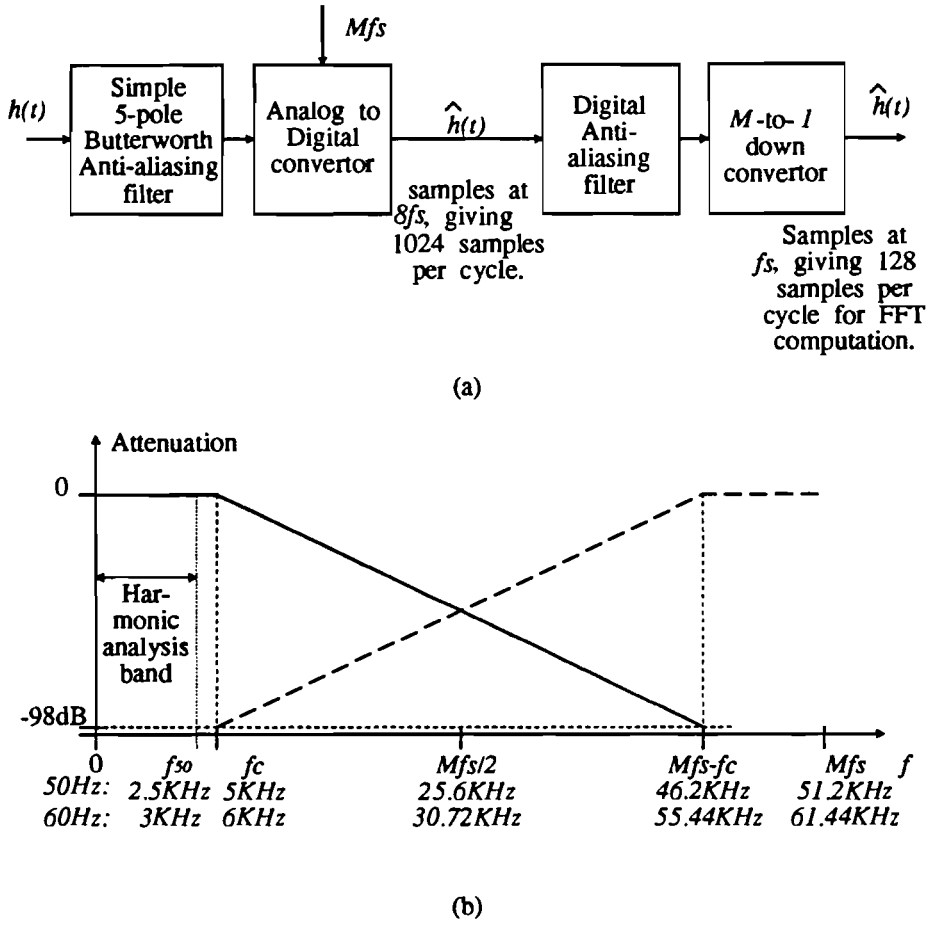


Figure 6.6 (a) Oversampling of a signal with anti-aliasing filtering performed by a digital filter. (b) The required filter response of an anti-aliasing filter preceding an oversampling ADC. Details for 50 Hz and 60 Hz power systems are shown below for an oversampling factor of $M = 8$.

$$y(n) = \sum_{k=0}^{N-1} h(k)x(n-k) \tag{6.9}$$

very efficiently [TI, 1986]. This is the direct-form structure of the N tap time-invariant FIR filter depicted in figure 6.7.

The frequency response of the filter required for anti-aliasing is depicted in figure 6.5(b). The filter coefficients, $h(k)$, were found from this response by essentially taking its inverse Fourier transform and modifying the resulting truncated impulse response by a Hamming window to reduce the Gibbs phenomenon [Crochiere and Rabiner, 1983]. The coefficients were then rounded for use in the 16 bit fixed point DSP [Chassaing and Horning, 1990]. The filter length was determined by two main factors, namely: the amount of processing time available on the DSP (the longer the filter the more processing is required), and how true the actual response is to be to the ideal response (the longer the filter, the better the response). The filter used in the CHART system has $N = 128$ taps, which is a good compromise between processing overhead and good response characteristics. Figure 6.8(a) shows the actual frequency magnitude response of the anti-aliasing

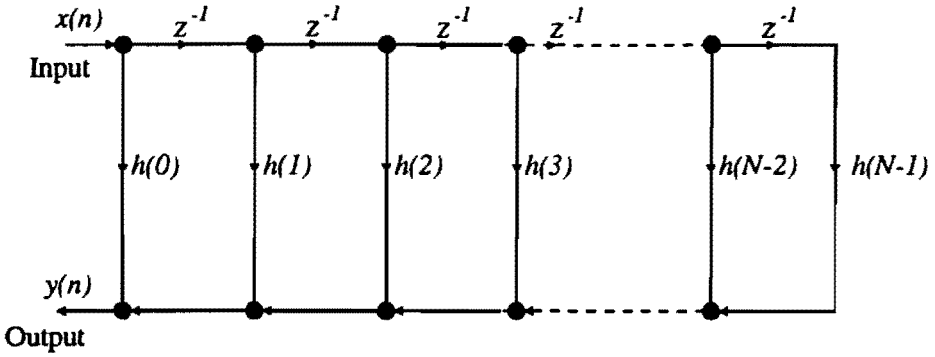


Figure 6.7 Direct form structure for a FIR digital filter.

FIR filter.

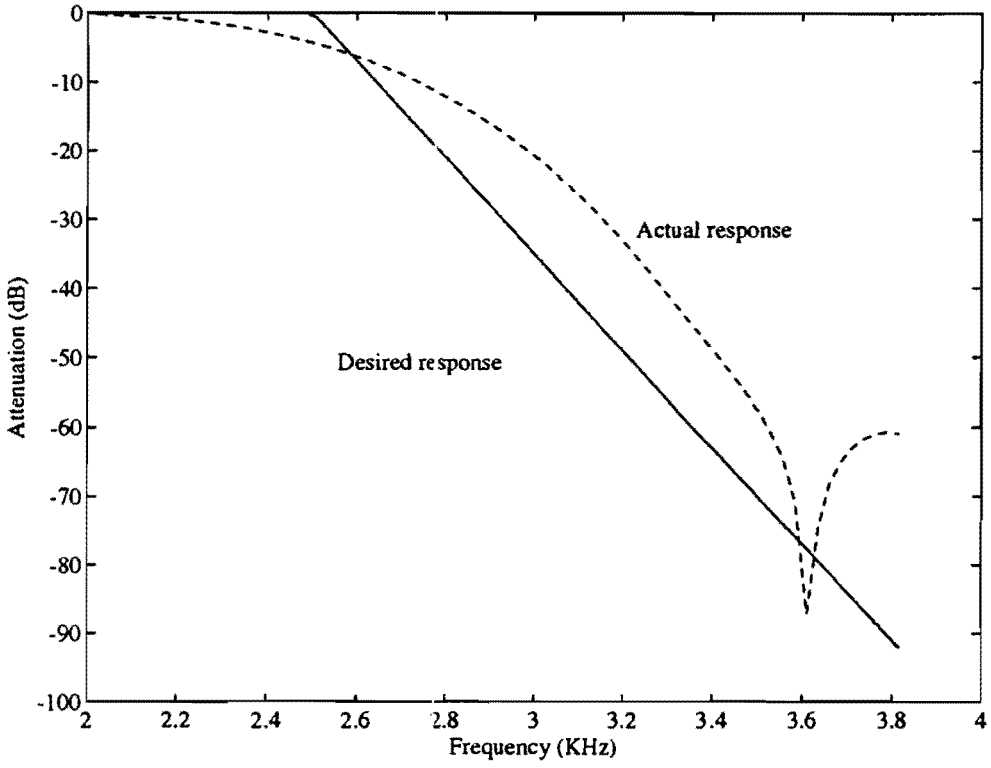


Figure 6.8 128-tap anti-alias FIR filter response for a 50 Hz fundamental (with rounded coefficients).

6.4 The FFT Record Length and Averaging

The frequency resolution of the FFT is given by the reciprocal of the time span that it is taken over (the record length),

$$\Delta f = \frac{1}{T_0}. \tag{6.10}$$

Hence to resolve harmonic values, separated by 50 Hz or 60 Hz, the record length must by one period of the fundamental frequency (20 mS or 16.7 mS). An FFT output bin is not however an impulse function centered on a particular harmonic. Instead it has a non zero response to frequencies between harmonics, as depicted in Figure 6.9. This means that signals present in the signal to be transformed that are not harmonics will contribute to particular harmonic outputs from the FFT, making them erroneous. The severity of this problem can be reduced by taking the FFT over longer time spans, thereby resolving inter-harmonic frequencies which would otherwise contribute to harmonic outputs. This does however require more processing of the data, as outlined in Table 6.1. In harmonic analysis this is seen as a disadvantage because only harmonics are required - as opposed to a spectrum analyzer which is required to have a very good resolution.

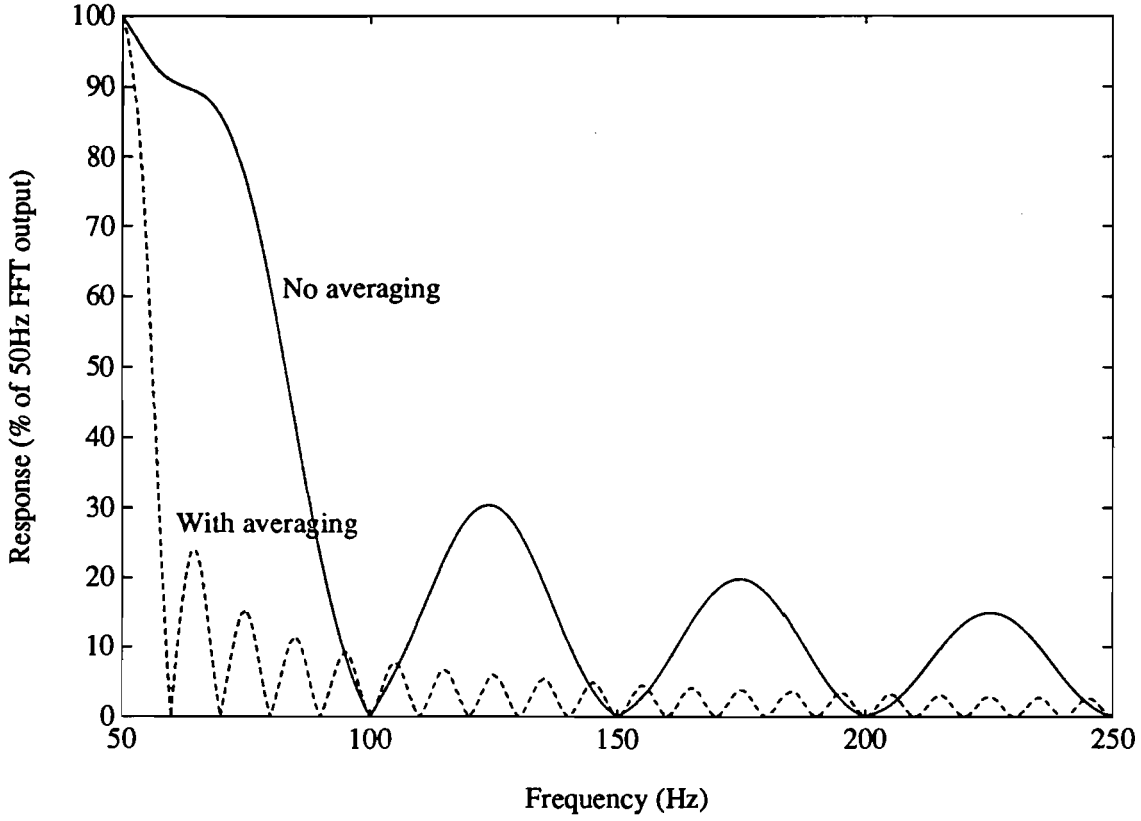


Figure 6.9 The response at the 50 Hz output bin of the FFT to a sine wave of higher frequency when sampling synchronously with 50 Hz over one cycle (averaging is over 5 cycles, with one resultant cycle).

It is possible to achieve the same effect of taking the FFT over several periods by averaging several periods to one and computing the FFT of that, provided that sampling is synchronous with the fundamental, as discussed in section 6.2.2. This preserves the bandwidth of the FFT with only a small processing overhead. The effect of averaging on the FFT response at 50Hz is also

FFT record length (N) samples	Time span (T_0)	Frequency resolution ($\Delta f = \frac{1}{T_0}$)	Number of instructions per second required to compute the FFT ($\frac{N^2}{log_2 N}/T_0$)
128	1 cycle = 20mS	50Hz	117,000
256	2 cycles = 40mS	25 Hz	204,800
512	4 cycles = 80mS	12.5 Hz	364,100
1024	8 cycles = 160mS	6.25 Hz	655,400
2048	16 cycles = 320mS	3.125 Hz	1,191,600

Table 6.1 Computation required for various length FFTs for a 50 Hz fundamental frequency

illustrated in Figure 6.9, and a derivation showing the effect of averaging 5 cycles to one and taking the DFT is given in Appendix 6C.

It must be noted that if sub-harmonics are required, averaging is not suitable. Instead the FFT must be taken over multiple cycles to produce the sub-multiples of the 50Hz or 60Hz fundamentals.

6.5 Implementation Details

6.5.1 The Anti-Aliasing FIR Filter

For a 50Hz fundamental frequency and an oversampling rate of $M = 8$, the ADC sampling rate is 51.2kHz[2]. To compute one output from the FIR filter of equation 6.9 requires N multiply and accumulate instructions, leading to $51.2 \times 128 = 6.5$ Million Instructions Per Second (MIPS) to implement the 128 tap filter. The TMS320C26 DSP is capable of a maximum of 10 MIPS [TI, 1986], and given that the 6.5 MIPS estimated to implement the 128 tap filter does not include any overhead, it is likely that the processor will not be able to complete an FFT in real-time after collecting 128 outputs from the filter. It must however be noted that the FIR filter is followed by an 8-to-1 decimator, meaning that the filter output need only be computed every 8th sample, theoretically reducing the MIPS required by the filter by a factor of 8 to less than 1 MIPS. Unfortunately this benefit is negated by the fact that the instruction set of the TMS320C26 DSP is arranged so that a multiply, accumulate, and shift is computed in one instruction, and although only every 8th sample requires a multiply and accumulate, all samples must be shifted in the filter shift register each time a new sample arrives - which happens at the higher sample rate.

Clearly a different approach is required to implement the filter efficiently. This approach involves breaking the filter up into a polyphase network, consisting of M smaller filters which contribute to the filter output for different time slots. The steps involved in forming a polyphase

[2]The required sampling rate for harmonic analysis up to the 50th harmonic is $2.56 f_{50} = 6.4$kHz from section 6.3. Multiplying this by 8 gives 51.2kHz.

network from a direct-form filter are illustrated diagrammatically in Figure 6.10 and are explained below.

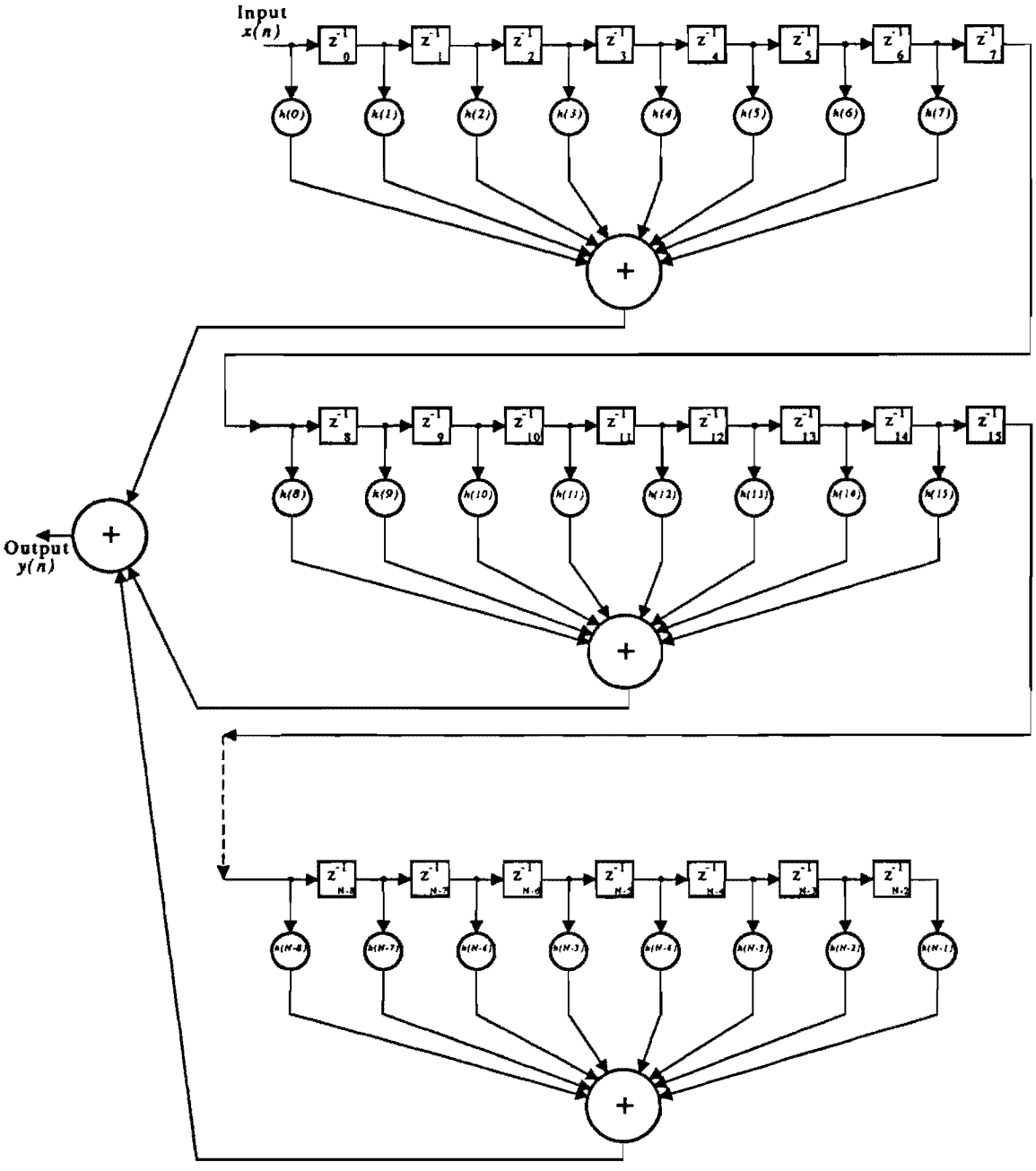


Figure 6.10 Direct form structure for a FIR digital filter arranged into columns so that when decimating by a factor of 8, each sample effectively moves down one row.

The direct-form structure of the time invariant FIR filter of Equation 6.9 is represented by Figure 6.10. This representation is used for simplicity in showing the transformation from the single phase filter to the poly-phase network. It has been established that the filter output, $y(n)$, need only be computed once for every M inputs, $x(n)$, for an M : 1 decimation. In the FIR filter implemented for the CHART project, an over sampling rate of $M = 8$ is employed. To produce

one output sample from Figure 6.10, 8 input samples are shifted into the filter shift register to occupy positions 0 to 7. After this an output is computed, and a further 8 samples are shifted in. The previous 8 samples are shifted to positions 8 to 15 and another output is computed. Shifting 8 inputs at a time in this manner can be avoided by forming the filter into the columns shown in Figure 6.10. From this it can be seen that position 0, for instance, need not be shifted all the way along the register to position 8, but can instead be shifted directly down to position 8. From this the filter can be transformed from a single N tap filter to M $\frac{N}{M}$ tap filters, where the output of only one filter need be computed for each input sample. This filter form is referred to as the *commutator model*, illustrated in figure 6.11 [Crochiere and Rabiner, 1983].

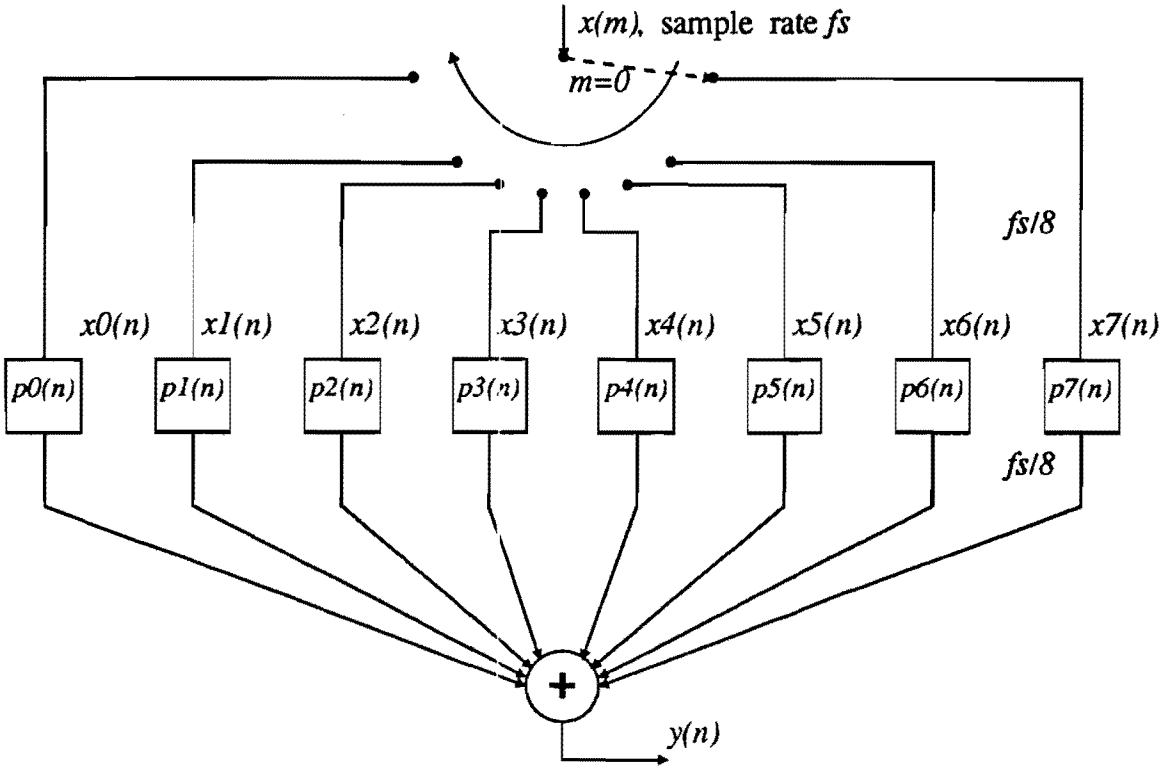


Figure 6.11 The commutator model for an 8-to-1 polyphase decimator. Each of the polyphase filters is a decimated version of the full filter impulse response $h(k)$.

The coefficients of the M-to-1 polyphase decimator are

$$P_\rho(n) = h(nM + \rho), \tag{6.11}$$

for $\rho = 0, 1, 2, ..., M - 1$, and all n, where ρ denotes the ρth polyphase filter. The commutator effectively takes M input samples of the signal $x(m)$ and distributes them to the polyphase branches in the reverse sequence $\rho = 7, 6, 5, ..., 0$. When each of the polyphase filters has received a new input, the polyphase filters are computed and their outputs summed to give a single output sample $y(n)$. This means that for each input sample (at a rate of f_s), only a 128/8 = 16 tap filter needs to be computed, leading to $51.2 \times 16 = 0.8$ MIPS, which is significantly lower than the 6.5 MIPS required to implement the full filter. There is however a slight overhead in the

implementation of the polyphase filter, although the DSP is quite capable of completing the FFT in the remaining time.

6.5.2 The FFT

As has already been discussed, the voltage and current signals are sampled coherently with the fundamental frequency, providing a finite set of samples in a form ready for analysis of spectral content by the DFT, using an FFT algorithm. They are also filtered sufficiently to ensure that aliasing will not distort spectral information, and decimated to a rate high enough to resolve up to the 50th harmonic, but not so high that unnecessary computation is performed in taking the FFT. The task of finding voltage and current harmonic levels is consequently a straight forward implementation of the FFT on the DSPs.

The most critical aspect is to ensure the integrity of the data as it flows through the system in real-time at multiple rates (illustrated in figure 6.12), and of the DSPs registers and accumulator as it switches between the filtering task and the FFT task.

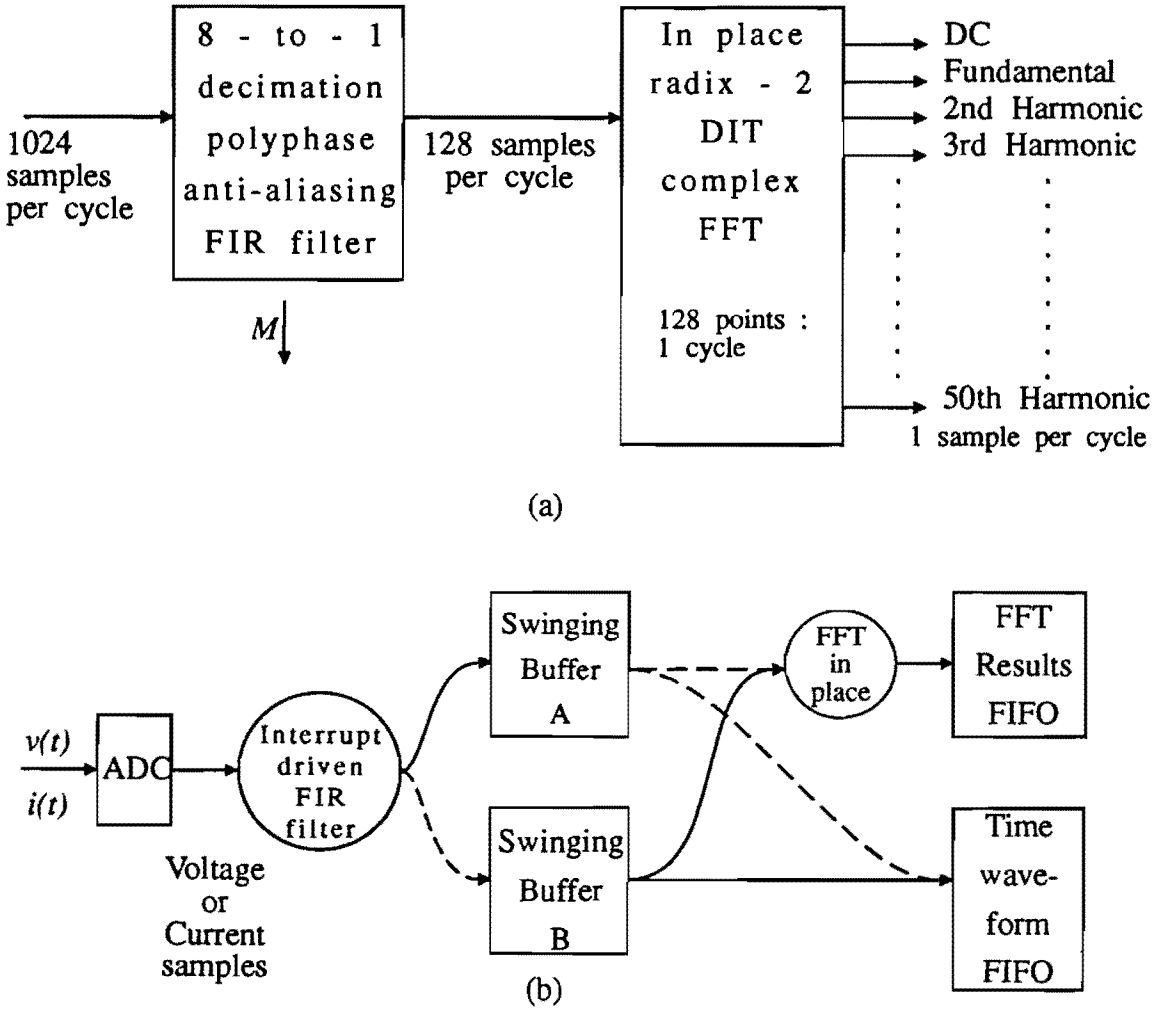


Figure 6.12 (a) Data flow in the DSP at various rates. (b) Data flow between tasks in the DSP.

Voltage and current signals acquired from transducers are real valued, which has two main implications. Firstly, the Fourier transform of the signals will have an even real part and an odd imaginary part, and secondly, it allows the butterfly operations in the first two stages of the FFT to be stream-lined by using only real arithmetic [Chassaing and Horning, 1990]. Algorithms do exist that implement an N point real FFT by weaving the real input data into an $N/2$ complex input array [Press *et al.*, 1989]. The DFT is therefore computed with an $\frac{N}{2}$ point complex FFT, although the only advantage of this is a saving in memory space, as the butterflies at each stage must be general complex ones, and the output must be decoded, leading to approximately the same processing requirements.

The CHART project uses a full 128 point complex FFT to compute the DFT, setting the complex inputs to zero before the transformation is started. Computation is performed in place and in internal RAM to save memory and for extra speed [TI, 1986]. Because the properties of the FFT output are known (due the input being real), only half the FFT output is required. A radix-2 algorithm [Brigham, 1974] is used, as the bit reversing required by this can be performed automatically by the CHART DSPs [TI. 1986], and a Decimation In Time (DIT) algorithm is used so that the input to the algorithm may be bit reversed, rather than the output. The complex FFT output is converted to polar form, giving harmonic magnitude and phase. This required the implementation of a square root algorithm and ARCTAN algorithm on the DSP.

Figure 6.12(a) illustrates the FIR filter task and the FFT task performed by each of CHARTs DSPs, and the data flow between them at multiple rates. The FIR filter decimates the oversampled input from 1024 samples per 50/60Hz cycle to 128 samples per cycle. Subsequent FFT analysis on each set of 128 samples leads to a set of harmonics updated each cycle, giving one of each of the 50 harmonics (magnitude and phase) per cycle[3]. The FIR filter is an interrupt driven task, with an operation by one of its polyphase filters performed each time a new sample arrives from the ADC (via the DSPs serial port). The FIR filter output is stored in one of the swinging buffers depicted in figure 6.12(b), leaving a buffer free for FFT analysis, thereby ensuring no loss of data between tasks. The FFT is performed on the data from the free buffer when the DSP is not in the FIR filter interrupt service routine, and its results (harmonics) are placed in a hardware FIFO buffer for use by the DAPMs host 80186 processor. The decimated time domain signal is also placed in a FIFO for use by the DAPMs host processor. A 'buffer swing' is performed once each cycle.

Each time an ADC sample arrives, the DSP must save its context from the FFT routine before servicing the sample and must restore the context before returning to the FFT. This adds a significant processing overhead to the DSP, as the ADC samples arrive at a high rate. Nevertheless, timing tests on the FIR filter and FFT operating independently and together indicate that the DSP is capable of implementing them in real-time. When performing a full context save and restore, the FIR filter takes 10ms to filter 1024 samples and produce 128 for the FFT. The FFT takes 2ms, including moving data from the swinging buffers into its in-place computation area (in the DSPs internal RAM), and moving the FFT results to the FIFO. The total time taken is therefore 12ms,

[3]If averaging is used, harmonics are computed per N averaged cycles, leading to 50 harmonics per N cycles. If the FFT is computed over N cycles, $50N$ harmonics and inter-harmonic components are produced per N cycles

corresponding to 72 percent of the available time for a 60Hz fundamental frequency, or 60 percent for a 50Hz fundamental.

6.6 Conclusion

The principles of filtering, sampling, and averaging power system voltage and current signals for harmonic analysis using the FFT have been established, and their application in the CHART instrument has been described. The use of powerful digital signal processors in this instrument has enabled the implementation of multirate DSP techniques, leading to simplifications in data acquisition hardware, improved signal quality, and reduced computational requirements by the rest of the system. The multirate DSP techniques involved the design of a polyphase decimation anti-aliasing FIR filter, and the implementation of an FFT algorithm.

The CHART II instrument is a very flexible one, allowing DSP software developed on a PC to be down-loaded to the DSPs with minimal effort. This enables other harmonic analysis techniques to be tested easily making the instrument a powerful research tool. The technique described in the implementation details section of this chapter is only one of many that could be used for harmonic analysis, although it was found to be a very successful compromise between data acquisition hardware complexity and processing requirements.

Immediate plans for the development of harmonic analysis software using CHART are to increase the FFT record length beyond 1 cycle to 2, 4, 8, and 16 cycles, enabling the determination of inter-harmonic frequencies as well as sub-harmonics. Other research activities with CHART involve its use in transient analysis, which requires sampling at even higher rates than those required for harmonic analysis, and using its DSPs to analyze transients on voltage and current waveforms.

The steep anti-aliasing filter roll offs described in this chapter are not necessarily required in practice, as it is unlikely that there will be signals of full power above the harmonic analysis band.

The material collected in this chapter has been used for a paper presented at the 1992 IEEE International Conference on Harmonics in Power Systems [Miller and Dewe, 1992b]. The paper has also been approved for publication in the transactions of the IEEE Power Engineering Society.

Appendix 6A The Fourier Transform of a Sampled Signal Truncated in Time

This appendix shows the derivation of Equation 6.6 in Section 6.2.2.

Consider

$$H'(f) = H(f) * \Delta_0(f) * T_0 \frac{sin(\pi T_0 f)}{\pi T_0 f} \tag{6.12}$$

which is the Fourier transform of the sampled and truncated signal $h(t)$ of Figure 6.3(c).

Now if $h(t)$ is periodic it can be represented by a Fourier series expansion, with Fourier transform given by the equation

$$H(f) = \sum_{n=0}^{\infty} \alpha_n \delta(f - nf_0), \tag{6.13}$$

where α_n are the complex Fourier series coefficients [Brigham, 1974].

If $h(t)$ is band-limited, this summation is over a finite number of harmonics from 0 to N (with the fundamental frequency equal to f_0). Substituting the Fourier transfrom of the bandlimited signal $H(f)$ into equation 6.12 yields

$$H'(f) = [\sum_{n=0}^{N} \alpha_n \delta(f - nf_0)] * \Delta_0(f) * \frac{T_0 sin(\pi T_0 f)}{\pi T_0 f}. \tag{6.14}$$

Now since $h(t)$ is band-limited, if the Nyquist sampling criteria of equation 6.4 is met (that is, if aliasing does not occur), the base band signal alone can be considered (since this contains all the information necessary to reconstruct $h(t)$).

Expanding out the convolution with $\Delta_0(f)$ yields a base band term and spectra repeated at integer multiples of f_s. The base band term is

$$H'(f) = f_s[\sum_{n=0}^{N} \alpha_n \delta(f - nf_0)] * \frac{T_0 sin(\pi T_0 f)}{\pi T_0 f}. \tag{6.15}$$

Convolving these two terms yields

$$\begin{aligned} H'(f) &= T_0 f_s \int_{-\infty}^{\infty} \sum_{n=0}^{N} \alpha_n \delta(\nu - nf_0) \frac{sin[\pi T_0(f - \nu)]}{\pi T_0(f - \nu)} d\nu \\ &= T_0 f_s \sum_{n=0}^{N} \alpha_n \frac{sin[\pi T_0(f - nf_0)]}{\pi T_0(f - nf_0)}, \end{aligned} \tag{6.16}$$

which is the Fourier transform of the bandlimited sampled and truncated signal.

Appendix 6B The Interference from an Adjacent Harmonic

This appendix gives the derivation of Equation 6.7 in Section 6.2.2.

The contribution of harmonic n_1 at harmonic n_2 is given by the evaluation of $H'_{n1}(f)$ at $f = n_2 f_0$,

$$H'_{n1}(n_2 f_0) = \alpha_{n1} T_0 f_s \frac{sin(\pi T_0 f_0 [n_2 - n_1])}{\pi T_0 f_0 [n_2 - n_1]} \tag{6.17}$$

from Equation 6.6 derived in Appendix 6A. If $T_0 f_0 \neq n$, where n is an integer, $H'_{n1}(n_2 f_0)$ will be non zero at n_2, with an attenuation given by

$$\begin{aligned} A &= \frac{H'_{n1}(n_2 f_0)}{H'_{n1}(n_1 f_0)} \\ &= \frac{sin(\pi T_0 f_0 [n_2 - n_1])}{\pi T_0 f_0 [n_2 - n_1]}. \end{aligned} \tag{6.18}$$

That is, the interference of a signal at harmonic n_1 on harmonic n_2 will have an attenuation A relative to the signal at n_1, which is dependent on the separation of the two harmonics, but more importantly on how close $T_0 f_0$ is to unity, or how close the truncation interval is to an integer multiple of the fundamental frequency.

The attenuation for adjacent harmonics (where $n_1 - n_2 = 1$) in dB is given by

$$A = 20 log_{10} \left| \frac{sin(\pi T_0 f_0)}{\pi T_0 f_0} \right|. \tag{6.19}$$

Appendix 6C The Effect on the Resultant DFT Spectrum of Averaging in the Time Domain

This appendix shows the effect on the resultant DFT spectrum of averaging 5 time domain cycles to one and computing the DFT of the resulting averaged cycle. The effect is shown by first sampling, truncating, and averaging in the time domain. The resulting function is then convolved in the time domain with the inverse Fourier transform of a frequency domain sampling function. The Fourier series of this is then found to give the DFT of the averaged function. It is included as supporting material for Section 6.4.

The sampled input of Figure 6.1(c) is represented by

$$h(t)\delta_0(t) = \sum_{k=-\infty}^{\infty} h(kT)\delta(t - kT), \tag{6.20}$$

where $\delta_0(t)$ is the sampling function,

$$\delta_0(t) = \sum_{k=-\infty}^{\infty} \delta(t - kT). \tag{6.21}$$

The sampled input multiplied by the rectangular truncation function $x(t)$, of Figure 6.3(b), where

$$x(t) = 1 \text{ for } \frac{-T}{2} < t < T_0 - \frac{T}{2},$$
$$x(t) = 0 \text{ otherwise}, \tag{6.22}$$

and T_0 is the period of $h(kT)$ gives the truncated input

$$h(t)\delta_0(t)x(t) = \sum_{k=0}^{N-1} h(kT)\delta(t - kT), \tag{6.23}$$

illustrated in Figure 6.3(c). Averaging the sampled and truncated input over 5 cycles gives

$$[h(t)\delta_0(t)x(t)]_{ave} = \frac{1}{5}\sum_{i=-2}^{2}[\sum_{k=0}^{N-1} h(kT + iT_0)\delta(t - kT + iT_0)]. \tag{6.24}$$

Expanding out the first summation gives

$$\begin{aligned}[h(t)\delta_0(t)x(t)]_{ave} = \frac{1}{5}\sum_{k=0}^{N-1}[&h(kT)\delta(t - kT)\\ &+h(kT + T_0)\delta(t - kT + T_0)\\ &+h(kT - T_0)\delta(t - kT - T_0)\\ &+h(kT + 2T_0)\delta(t - kT + 2T_0)\\ &+h(kT - 2T_0)\delta(t - kT - 2T_0)].\end{aligned} \tag{6.25}$$

If we assume that $h(kT)$ remains the same over all five periods, ie. $h(kT) = h(kT + T_0) = h(kT - T_0) = h(kT + 2T_0) = h(kT - 2T_0)$, $h(kT)$ becomes a common factor, giving

$$[h(t)\delta_0(t)x(t)]_{ave} = \frac{1}{5}\sum_{k=0}^{N-1} h(kT)[\delta(t - kT) + \delta(t - kT \pm T_0) + \delta(t - kT \pm 2T_0)]. \tag{6.26}$$

This assumes that the magnitude of $h(kT)$ does not vary with time over the five cycles.

The Fourier transform of this must be sampled (in the frequency domain) to convert it to the discrete Fourier transform by multiplying by the Fourier transform of

$$\delta_1(t) = T_0 \sum_{r=-\infty}^{\infty} \delta(t - rT_0) \tag{6.27}$$

in the frequency domain [Brigham, 1974].

This is a convolution in the time domain,

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$$\begin{aligned}\bar{f}(t)_{ave} &= [h(t)\delta_0(t)x(t)]_{ave} * \delta_1(t) \\ &= \frac{1}{5}\sum_{k=0}^{N-1} h(kT)[\delta(t-kT) + \delta(t-kT\pm T_0) + \delta(t-kT\pm 2T_0)] \\ &\quad * T_0 \sum_{r=-\infty}^{\infty} \delta(t-rT_0)\end{aligned} \tag{6.28}$$

Expanding this gives

$$\begin{aligned}\bar{f}(t)_{ave} = \cdots &+ \frac{1}{5}T_0\sum_{k=0}^{N-1} h(kT)\delta(t-kT+T_0) \\ &+ \frac{1}{5}T_0\sum_{k=0}^{N-1} h(kT)\delta(t-kT) \\ &+ \frac{1}{5}T_0\sum_{k=0}^{N-1} h(kT)\delta(t-kT-T_0) + \cdots \\ \cdots &+ \frac{1}{5}T_0\sum_{k=0}^{N-1} h(kT)\delta(t-kT\pm T_0+T_0) \\ &+ \frac{1}{5}T_0\sum_{k=0}^{N-1} h(kT)\delta(t-kT\pm T_0) \\ &+ \frac{1}{5}T_0\sum_{k=0}^{N-1} h(kT)\delta(t-kT\pm T_0-T_0) + \cdots \\ \cdots &+ \frac{1}{5}T_0\sum_{k=0}^{N-1} h(kT)\delta(t-kT\pm 2T_0+T_0) \\ &+ \frac{1}{5}T_0\sum_{k=0}^{N-1} h(kT)\delta(t-kT\pm 2T_0) \\ &+ \frac{1}{5}T_0\sum_{k=0}^{N-1} h(kT)\delta(t-kT\pm 2T_0-T_0) + \cdots\end{aligned} \tag{6.29}$$

Which has the general expression

$$\begin{aligned}\bar{f}(t)_{ave} = \frac{1}{5}T_0\sum_{r=-\infty}^{\infty}\Bigg[\sum_{k=0}^{N-1} h(kT)[&\delta(t-kT-rT_0) \\ &+\delta(t-kT\pm T_0-rT_0) + \delta(t-kT\pm 2T_0-rT_0)]\Bigg].\end{aligned} \tag{6.30}$$

This is a periodic function with period T_0, with each period consisting of N samples.

The Fourier series for this periodic function is represented by

$$\tilde{F}(\frac{n}{T_0})_{ave} = \sum_{n=-\infty}^{\infty} \alpha_n \delta(f - nf_0), \text{ where } f_0 = \frac{1}{T_0}, \tag{6.31}$$

with the complex Fourier coefficients given by

$$\alpha_n = \frac{1}{T_0}\int_{\frac{-T}{2}}^{T_0-\frac{T}{2}} \tilde{f}(t)_{ave} e^{-j2\pi n\frac{t}{T_0}} dt, \text{ for } n = 0, \pm 1, \pm 2, \cdots \tag{6.32}$$

Substituting $\tilde{f}(t)_{ave}$ from Equation 6.30 into this gives

$$\alpha_n = \frac{1}{T_0}\frac{1}{5}\int_{\frac{-T}{2}}^{T_0-\frac{T}{2}} T_0 \sum_{r=-\infty}^{\infty} \Big[\sum_{k=0}^{N-1} h(kT)[\delta(t - kT - rT_0) + \delta(t - kT \pm T_0 - rT_0) + \delta(t - kT \pm 2T_0 - rT_0)]\Big] e^{-j2\pi n\frac{t}{T_0}} dt. \tag{6.33}$$

Integration is only over one period, hence the summation $\sum_{r=-\infty}^{\infty}$ can be dropped, yielding

$$\alpha_n = \frac{1}{5}\int_{\frac{-T}{2}}^{T_0-\frac{T}{2}} \sum_{k=0}^{N-1} h(kT)[\delta(t - kT) + \delta(t - kT \pm T_0) + \delta(t - kT \pm 2T_0)] e^{-j2\pi n\frac{t}{T_0}} dt. \tag{6.34}$$

Expanding this out gives

$$\begin{aligned}
\alpha_n &= \frac{1}{5}\sum_{k=0}^{N-1} h(kT)\int_{\frac{-T}{2}}^{T_0-\frac{T}{2}} e^{-j2\pi n\frac{t}{T_0}}\delta(t - kT)dt \\
&\quad + \frac{1}{5}\sum_{k=0}^{N-1} h(kT)\int_{\frac{-T}{2}}^{T_0-\frac{T}{2}} e^{-j2\pi n\frac{t}{T_0}}\delta(t - kT \pm T_0)dt \\
&\quad + \frac{1}{5}\sum_{k=0}^{N-1} h(kT)\int_{\frac{-T}{2}}^{T_0-\frac{T}{2}} e^{-j2\pi n\frac{t}{T_0}}\delta(t - kT \pm 2T_0)dt \\
&= \frac{1}{5}\sum_{k=0}^{N-1} h(kT)e^{-j2\pi nk\frac{T}{T_0}} + \frac{1}{5}\sum_{k=0}^{N-1} h(kT)\int_{\frac{-T}{2}}^{T_0-\frac{T}{2}} [e^{-j2\pi n\frac{t}{T_0}}\delta(t - kT - T_0) \\
&\quad + e^{-j2\pi n\frac{t}{T_0}}\delta(t - kT + T_0) + e^{-j2\pi n\frac{t}{T_0}}\delta(t - kT - 2T_0) \\
&\quad + e^{-j2\pi n\frac{t}{T_0}}\delta(t - kT + 2T_0)] \\
&= \frac{1}{5}\sum_{k=0}^{N-1} h(kT)[e^{-j2\pi nk\frac{T}{T_0}} \\
&\quad + e^{-j2\pi n\frac{kT+T_0}{T_0}} + e^{-j2\pi n\frac{kT-T_0}{T_0}} \\
&\quad + e^{-j2\pi n\frac{kT+2T_0}{T_0}} + e^{-j2\pi n\frac{kT-2T_0}{T_0}}] \\
&= \frac{1}{5}\sum_{k=0}^{N-1} h(kT)e^{-j2\pi nk\frac{T}{T_0}}[1 + e^{-j2\pi n} + e^{+j2\pi n} + e^{-j2\pi n(2)} + e^{+j2\pi n(2)}].
\end{aligned} \tag{6.35}$$

Representing the exponential terms as cosine terms, gives

$$\alpha_n = \frac{1}{5}\sum_{k=0}^{N-1} h(kT)e^{-j2\pi n\frac{kT}{T_0}}[1 + 2cos(2\pi n) + 2cos(4\pi n)],$$
$$n = 0, \pm 1, \pm 2, \cdots \tag{6.36}$$

Now $T_0 = NT$, therefore

$$\alpha_n = \frac{1}{5}\sum_{k=0}^{N-1} h(kT)e^{-j2\pi n\frac{k}{N}}[1 + 2cos(2\pi n) + 2cos(4\pi n)]. \tag{6.37}$$

Substituting this into the Fourier series of equation 6.31 gives

$$\tilde{F}(\frac{n}{NT})_{ave} = \frac{1}{5}\sum_{n=-\infty}^{\infty}\left[\sum_{k=0}^{N-1} h(kT)e^{-j2\pi n\frac{k}{N}}[1 + 2cos(2\pi n) + 2cos(4\pi n)]\right]\delta(f - nf_0), \tag{6.38}$$

because $T_0 = NT$.

If we let $n = r$ where r is an arbitrary integer, we obtain the discrete Fourier transform for the averaged cycle,

$$\tilde{F}(\frac{r}{NT})_{ave} = \frac{1}{5}\sum_{k=0}^{N-1} h(kT)e^{\frac{-j2\pi rk}{N}}[1+2cos(2\pi r)+2cos(4\pi r)], \text{ for } r = 0, 1, ..., N-1 \tag{6.39}$$

for harmonic of order r. This is the DFT given by equation 6.1 modified by the term

$$m(r) = \frac{1}{5}[1 + 2cos(2\pi r) + 2cos(4\pi r)], \tag{6.40}$$

which has maxima at integer values of r. To represent non harmonic frequencies, r is given a real value between harmonics. For instance $r = 1.2$ to represent 60Hz for a 50Hz fundamental. Plotting $m(r)$ out between the fundamental and second harmonic illustrates its effect on the DFT response to non harmonic signals, as depicted in Figure 6.13.

Averaging a number of time domain cycles to one reduces the response of the DFT to non harmonic signals at each harmonic. Specifically, averaging 5 cycles to one completely nulls the response at multiples of 10Hz as shown in Figure 6.13.

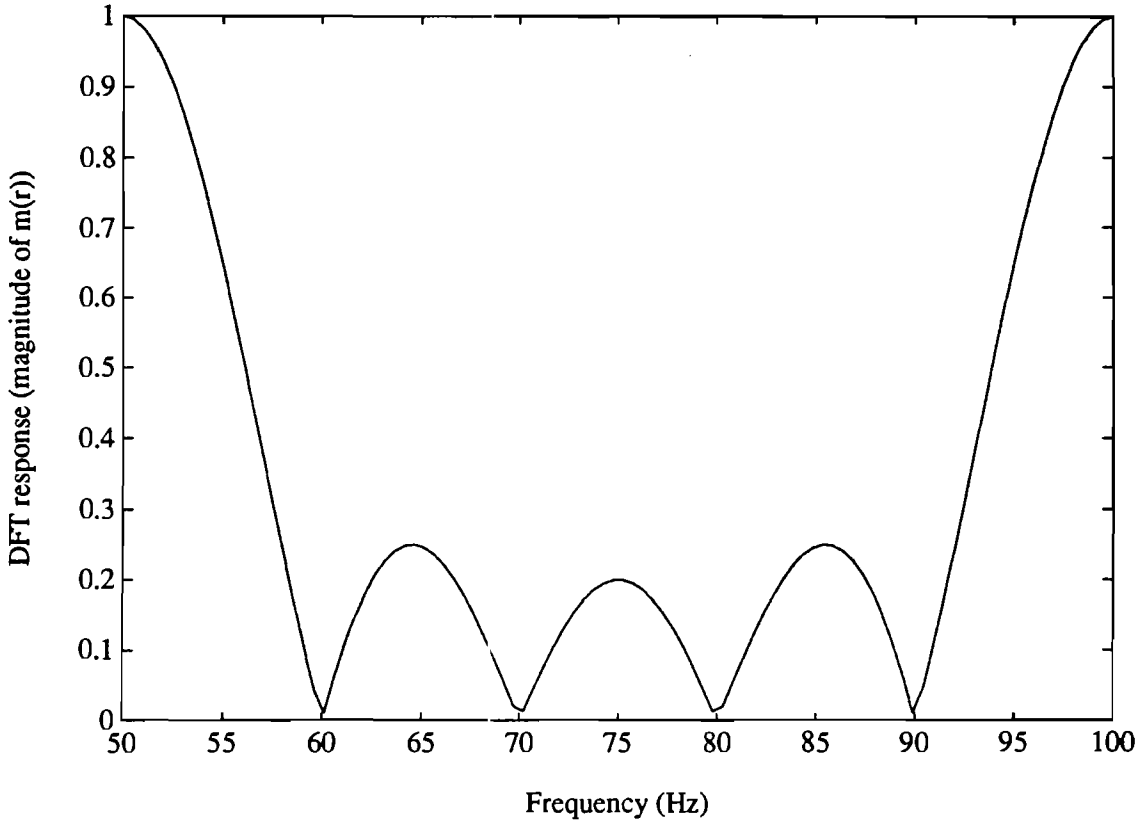

Figure 6.13 The effect on the resultant DFT spectrum of averaging in the time domain. r = Frequency /50.

Chapter 7

HARMONIC MEASUREMENTS ON THE NEW ZEALAND HVDC LINK USING CHART II

7.1 Introduction

In 1990 an upgrade to the New Zealand HVdc link between Benmore power station in the South Island and Haywards sub-station in the North Island began. The upgrade was achieved by paralleling both poles of the existing 600 MW Mercury-arc converter HVdc link, and adding a new 700 MW pole consisting of thyristor convertors. The configuration of the new system is illustrated in Figure 7.1, with ratings given in Table 7.1.

Pole	Nominal voltage (kV)	Nominal current (amps.)	Nominal power MW	Overload voltage (kV)	Overload current (amps.)	Overload power MW
Pole 1 Mercury-arc	+270 kV	1600 A	432 MW	+270 kV	2000 A	540 MW
Pole 2 Thyristor	-350 kV	1600 A	560 MW	-350 kV	2000 A	700 MW

Table 7.1 The upgraded New Zealand inter island HVdc link ratings.

It is clear from Table 7.1 and Figure 7.1 that the new transmission system is asymmetrical, with pole 2 rated at a higher power and voltage than pole 1, but with the same current rating to avoid ground return currents. As part of the commissioning tests for the new pole (pole 2), the harmonics generated by it were required to be measured to verify the effectiveness of the pole 2 ac harmonic filters, and to ensure that harmonic levels are within the limits specified in the contract specification [ABB, 1989]. These tests were performed on the 14th, 15th, and 30th of October, 1992 at Benmore power station, and on the 6th of November at the Haywards substation. The CHART II harmonic monitor was used to monitor, analyze, and record harmonic levels throughout the tests. The Design Power NOWA 1 Harmonic monitoring equipment, and the HP

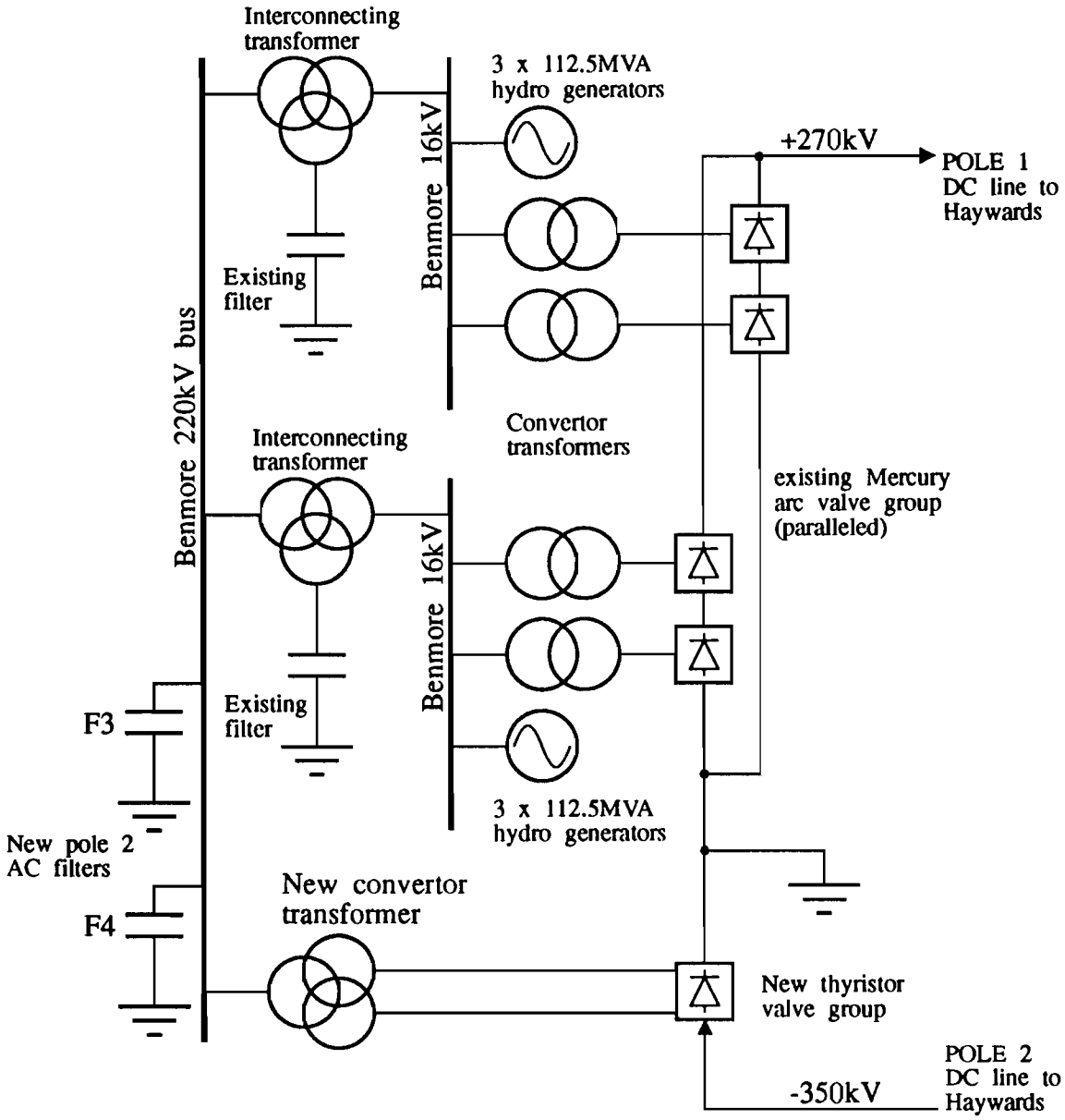

Figure 7.1 The Benmore terminal of the upgraded HVdc link

data acquisition system owned by Transpower New Zealand Limited were also used. The primary purpose for using CHART II in these tests was as a field trial to evaluate its performance in a realistic environment, to demonstrate its capabilities, and to compare it with existing harmonic monitoring equipment. This chapter documents part of the harmonic tests, covering the connection of CHART to the high voltage network and CHARTs configuration, a summary of the DC1 specification which sets limits for all harmonic levels from the new convertor arrangement, and the procedure and results from one of the tests.

7.2 The Connection of CHART II to the High Voltage Network

The instrumentation windings of conventional metering CTs, which are part of existing installed equipment, were used to measure the current in each phase flowing into the converter transformer. The secondary windings of these transformers were terminated in 15 Ω burden resistors, which are part of Design Power New Zealand's harmonic monitoring equipment, as illustrated in Figure 7.2(a).

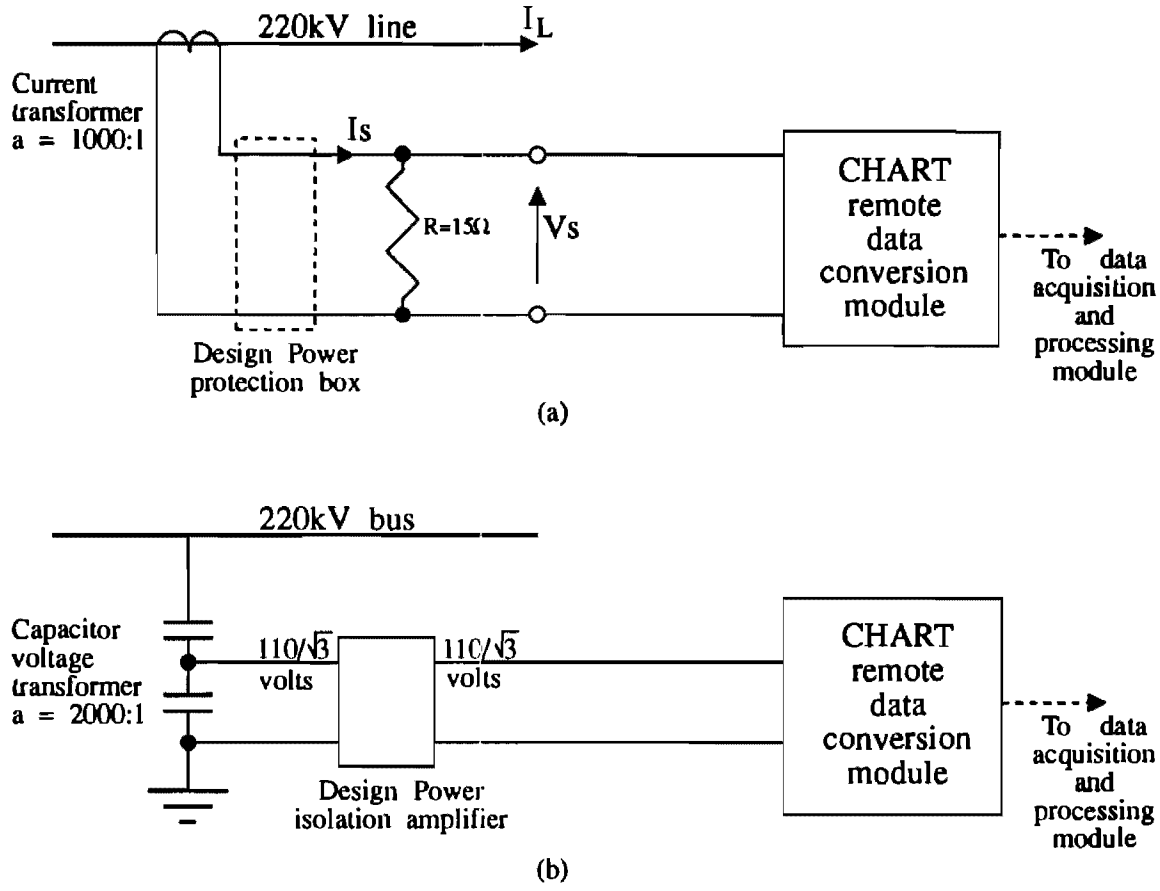

Figure 7.2 The connection of CHART to the high voltage network. (a) Current measurement. (b) Voltage measurement.

Remote data conversion modules were used to convert the voltage across the resistor illustrated in Figure 7.2 to digital samples which were transmitted to the CHART parallel processing unit by fibre optic cables, as discussed in Chapter 5. The line current is found from these samples representing V_s by

$$I_L = \frac{a}{R} V_s, \tag{7.1}$$

where a is the CT ratio (1000:1 for the single pole tests and 2400:1 for the bipole tests), and R is the CT burden resistor value.

Although the CHART instrument has the ability to compensate for non uniform CT magnitude

and phase frequency responses, no compensation for computed harmonic currents was made, as no data regarding the CTs used was available. The assumption that the CT frequency response is uniform is however valid for all frequencies below 5 KHz [Meynaud, 1989].

Measurement of the 220 kV bus harmonic voltage using conventional VTs is highly inaccurate, as these have resonant points in the frequency range of interest [Meynaud, 1989]. Although research into the determination of VT frequency response characteristics has been carried out [Bradley *et al.*, 1985a], no complete data of VT responses exist, making it impossible to compensate computed harmonic voltages for the transducer characteristics. Transpower New Zealand own a set of three harmonic measurement VTs for use in harmonic voltage measurements of three phase power systems. These have uniform magnitude frequency responses in the harmonic analysis band up to the 50th harmonic, and were installed on the 220 kV bus at each site especially for the tests. CHART II was connected to these as shown in Figure 7.2(b). The harmonic measurement CVTs have a 2000:1 ratio, giving a nominal output of 110 Vrms phase-to-phase from the 220 kV bus bar.

7.3 The Configuration of CHART for testing

To monitor 3 phase current and voltage, 3 DAPMs were used, with each DAPM used to monitor one voltage channel and one current channel. During these tests the SRM was not required, as the fundamental frequency was maintained within the limits set out in New Zealand legislation [NZED, 1983] during the intervals between load changing, meaning that spectral leakage from the FFT was not significant at these times. However, while changing the load, the system frequency may have exceeded the specified bounds, meaning that the FFT results may be erroneous during these 'transient' times. They are however very short in relation to the intervening intervals of constant load. One of the reasons for holding the DC link at a constant load was to allow the system frequency to stabilize.

The acquired data was passed through the FIR filter and averaged from four cycles to one (thereby complying with New Zealand legislation [NZED, 1983]), with the FFT taken over the averaged cycle, as discussed in Section 6.4. The FFT output data was transformed from complex Cartesian form to polar coordinate form. The averaged time domain cycle, and magnitude and phase FFT results were passed from each DSP to their host 80186 on the DAPM. A very simple on-line analysis algorithm was implemented on this to reduce the amount of data forwarded to the 486/133SE to be stored. This on-line analysis method simply looks at the fundamental current magnitude over a period of ten seconds, and stores both the voltage and current channels' data corresponding to the maximum fundamental current. It then message passes this harmonic data to the 486/133SE which operates a task for each DAPM that stores the received data to hard disk, as well as time and date stamping it. Current was monitored instead of voltage, as this changes continuously over a wide range, whereas voltage varies only slightly. The on-line analysis method is illustrated in Figure 7.3.

It was realized after the tests that the on-line analysis method used requires some refinement if the harmonic phase results from the FFT are to be compared between the three power system

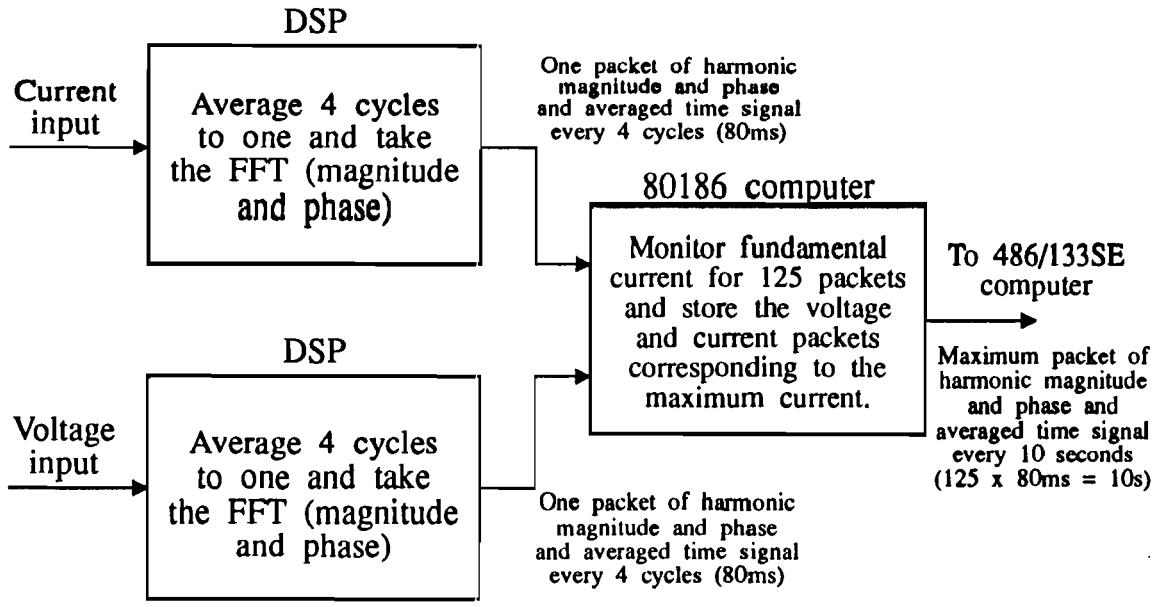

Figure 7.3 The on-line harmonic analysis performed by CHART II's DAPMs for pole 2 commissioning tests.

phases. This is because the maxima on each phase do not necessarily occur simultaneously, meaning that the data stored may not correspond in time between the three phases. Nevertheless, the phase responses of the CTs and VTs were unknown, so it was not possible in this case to compare phases between voltage and current accurately at harmonic frequencies.

As discussed in section 5.3, data to the display PC was retrieved from the data stored on hard disk by a task operating on the 486/133SE. A temporary serial link (using RS232) from the 486/133SE computer to the display PC was used to transfer data between them. The data was multiplied by the appropriate scaling factors on the PC to convert it into real quantities - namely RMS amperes for current and percentage of the fundamental voltage for voltage.

7.4 Summary of the DC1 Specification

The DC1 specification gives individual harmonic current and voltage limits, as well as THD, EDV, and EDI limits for the new convertor arrangement. These parameters are defined in Section 2.2.1, and their limits are listed in tables 7.2 and 7.3.

7.5 Pole 2 Harmonic Tests

Three pole 2 harmonic tests were performed at Benmore power station, and one at Haywards substation. Of the three tests carried out at Benmore, two involved operating pole 2 without pole 1; one at its full voltage, and the other at its reduced voltage. The third test at Benmore was a bipole test, with both poles operating. The test at Haywards substation was a bipole test. Only the 'pole 2 at full voltage' test is documented here for the purpose of illustrating what data was recorded during the tests and how it is presented in a concise manner.

Odd Harmonics	U_n limit (% of fundamental)	I_n limit (amperes at 1pu system voltage)
3	2.3	57
5	1.4	34
7	1.0	25
9	0.8	19
11	0.7	16
13	0.6	14
15	0.5	12
17	0.4	10
19 and 21	0.4	9
23	0.3	8
25 to 49	0.3	7
Even Harmonics	**U_n limit (% of fundamental)**	**I_n limit (amperes at 1pu system voltage)**
2	1.2	29
4	0.6	15
6	0.4	10
8	0.3	8
10	0.3	6
12 and 14	0.2	5
16 and 18	0.2	4
20 to 50	0.2	3

Table 7.2 DC1 Specification individual harmonic voltage distortion (U_n) limits on the Benmore 220 kV bus, and individual harmonic current (I_n) limits flowing into the 220 kV system at Benmore.

Parameter	Limit
EDI	26 amperes
EDV	1.0 %
THD	3.0 %

Table 7.3 Equivalent disturbing current (EDI) limit flowing into the 220 kV system at Benmore, equivalent disturbing voltage (EDV) limit on the Benmore 220 kV buses, and total harmonic distortion (U_t or THD) limit on the Benmore 220 kV buses.

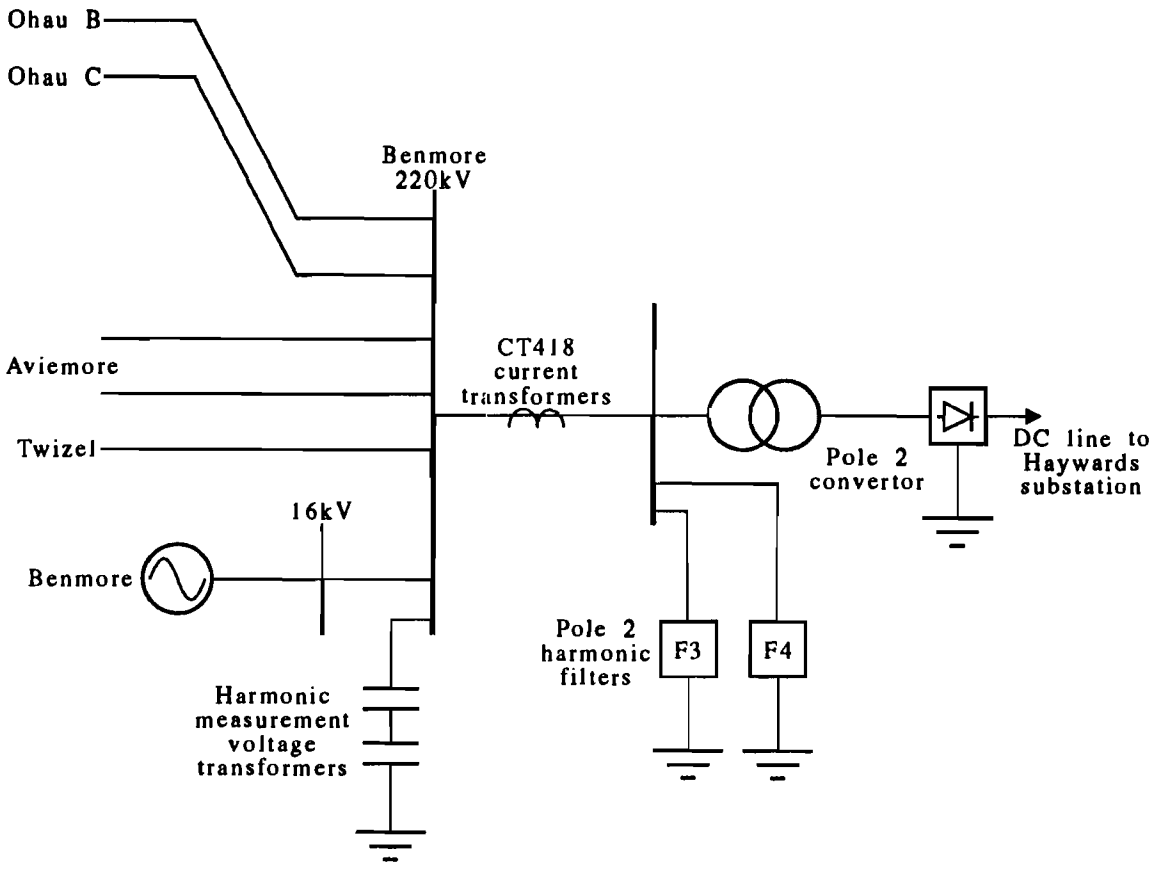

Figure 7.4 Measurement of harmonic voltage and current for Test 1.

7.5.1 Benmore Pole 2 Full Voltage Test Procedure

The purpose of this test was to examine the effectiveness of the pole 2 ac harmonic filters at various loads transferred on pole 2 of the dc transmission system with only pole 2 operating. Pole 2 was operated at its full voltage. Harmonic currents injected into the 220kV system at Benmore from the pole 2 convertor acting as a rectifier were measured using CT418 shown in Figure 7.4. The Transpower harmonic measurement CVTs were connected to the Benmore 220kV bus.

Throughout this test, pole 1 and its harmonic filters were left off to minimize background harmonic levels. Before the test began, background harmonic levels were recorded. At the start of the test, pole 2 was started and ramped up to full power in stages, allowing harmonic levels to be measured at various power levels. At full power the ac harmonic filter F4 was switched out and pole 2 was ramped down and stopped. The power profile for pole 2 for this test is depicted in Figure 7.5

7.5.2 Benmore Pole 2 Full Voltage Test Results

To present the complete results of monitoring the three voltage channels and the three current channels requires 300 graphs of harmonic magnitude versus time[1]. In addition to this, THD,

[1]There are 50 harmonics per channel, and 6 channels, which equates to 300 graphs.

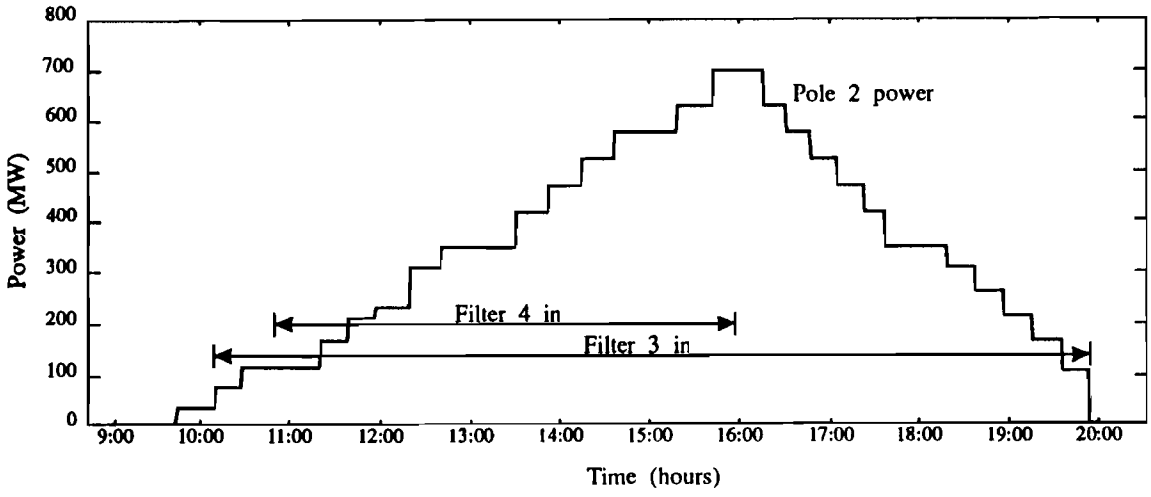

Figure 7.5 Pole 2 power profile for Test 1.

EDV, and EDI per phase versus time are required, leading to a tremendous amount of data for graphical presentation. However only the data of interest (harmonics that are close to their limits for instance) need to be graphed. This reduces the quantity of data to a manageable size. To find only significant data from the stored harmonics, each harmonic for each channel was compared with its limit set out in the DC1 specification, summarised in Section 7.4, and the percentage of time that the harmonic exceeded 90% of its limit was computed. These results are a shown in Table 7.4 and Table 7.5. In addition to these, THD, EDV, and EDI were computed and compared with the limits, with the results shown in Table 7.6.

Harmonic	percentage of time above 90% of the limit		
	Red phase	Yellow phase	Blue phase
2 and 3	0	0	0
4	14.4	12.6	16.5
5 to 50	0	0	0

Table 7.4 Voltage harmonics measured during the pole 2 full voltage test on October 14, 1992.

Tables 7.4, 7.5, and 7.6 show that only the 3 phases of 4th harmonic current and voltage exceeded 90% of their respective limits. Further investigation showed that they actually exceeded the full limit. To determine under what conditions the limits were exceeded, each phase was graphed against time, with the power profile of the test superimposed on it to identify the stages of the test. The Red phase 4th harmonic is shown in Figure 7.6. Figure 7.6(a) clearly shows that the 4th harmonic voltage exceeds it limit when pole 2 is near its maximum rating and when both filters are operating. It also shows that the 4th harmonic voltage drops significantly when one of the harmonic filters is switched out. This indicates a possible resonant frequency at the 4th

Harmonic	percentage of time above 90% of the limit		
	Red phase	Yellow phase	Blue phase
2 and 3	0	0	0
4	1.9	10.3	3.4
5 to 50	0	0	0

Table 7.5 Current harmonics measured during the pole 2 full voltage test on October 14, 1992.

Parameter	percentage of time above 90% of the limit		
	Red phase	Yellow phase	Blue phase
EDI	0	0	0
EDV	0	0	0
THD	0	0	0

Table 7.6 Harmonics measured during the pole 2 full voltage test on October 14, 1992.

harmonic when both filters are operating, which shifts to a higher resonant frequency when one filter is removed. Figure 7.6(b) shows that the 4th harmonic current approaches its limit, almost exceeding it. Again it drops significantly when one harmonic filter is switched out. No excessive 4th harmonic levels were found in the bipole tests, indicating that the 4th harmonic is a by-product of operating the link with only one pole, and is amplified by a resonant condition. To present a cross section of data produced by CHART, EDI, EDV, and THD computed during the test are shown in Figure 7.7, together with the test power profile and filter switching information.

A feature of CHART is that the time domain cycle corresponding to a set of harmonics is stored in addition to the harmonics. The Red phase time domain cycles corresponding to the maximum 4th harmonic voltage in Figure 7.6 are shown in Figures 7.8 and 7.9, with their harmonic spectrum.

7.6 Conclusion

During the first two tests at Benmore, Transpower found inter-harmonic frequency components at 125 Hz, 175 Hz, and 375 Hz from $\frac{1}{2}$ second snapshots of data captured using their HP data acquisition system. The DFT of this data was found after its capture using MATLAB. These components were supressed by CHART as a consequence of averaging, as discussed in section 6.4. The discovery of these inter-harmonics highlights a limitation of harmonic analysis and suggests that for future measurements, longer FFT record lengths should be taken by CHART to resolve any

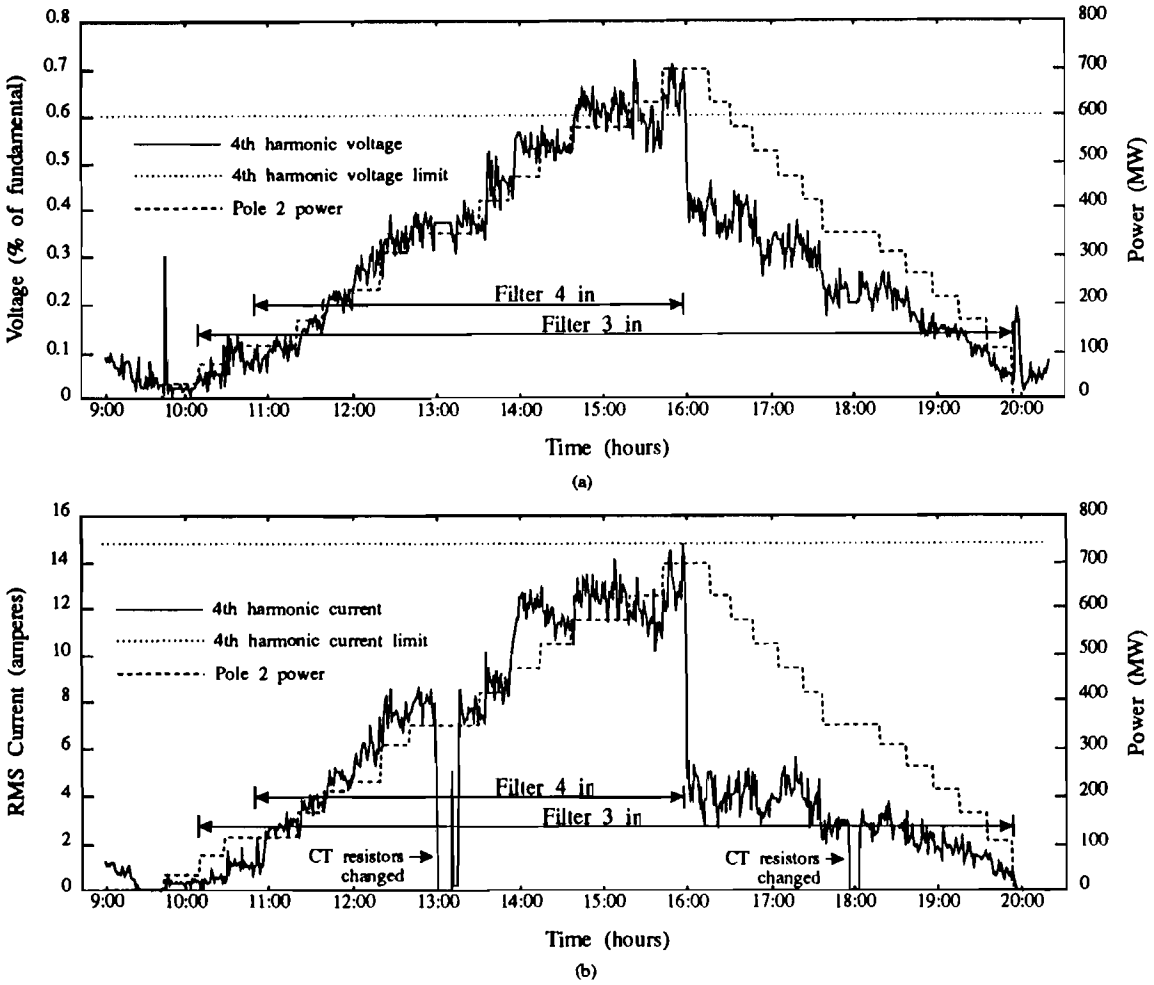

Figure 7.6 Red phase fourth harmonic measured during the pole 2 full voltage test on October 14, 1992: (a) Voltage, and (b) Current.

inter-harmonic signals that may be present instead of averaging to suppress them. A frequency resolution of 3.125 Hz can be achieved by CHART by taking the FFT over 16 cycles. This requires a change to the DSP software, but no fundamental system change. To be able to classify harmonics into sequence components (positive, negative, or zero sequence) is important for analysis and identification of the cause of the measured harmonics. This requires phase information, as well as magnitude information. Although CHART does find the harmonic phase, no data is available regarding the phase responses of CTs and VTs, which will distort the phase of the measured harmonics. This phase distortion can be compensated for in the frequency domain if the transducer phase responses are known. Ways of measuring the phase response of CVTs must be developed to enable harmonic phase to be used. This could be carried out in conjunction with measurement of conventional protection CVT magnitude responses to enable 'in house' CVTs to be used for harmonic measurement rather than shipping special CVTs around the country and installing them specifically for harmonic measurements.[2]

[2]Measurement of CVT responses up to the 50th harmonic is actually very difficult. This is due to non linearities caused by saturation of the magnetic core of the transformer on the CVT output, which makes the response of a CVT

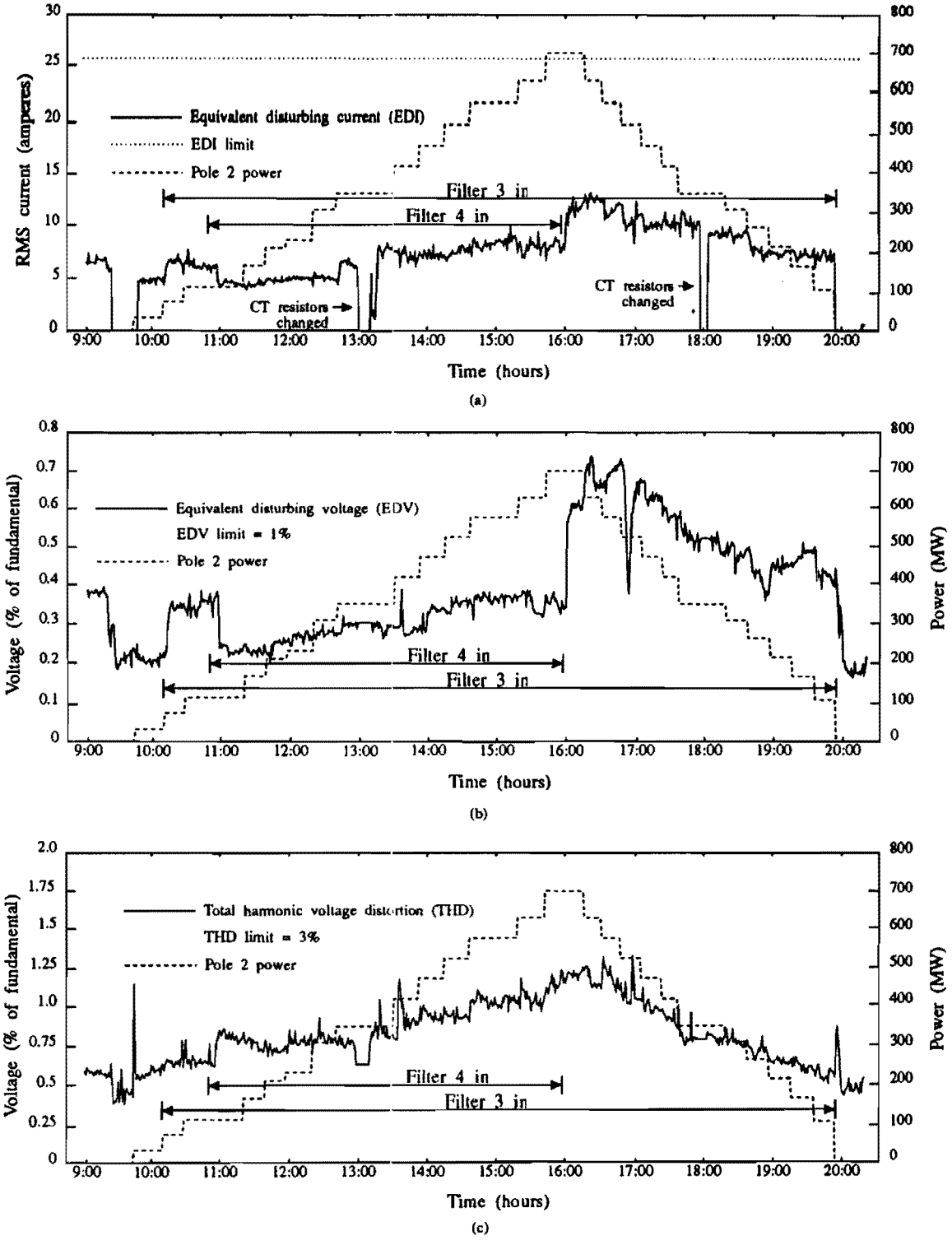

Figure 7.7 Red phase fourth harmonic measured during the pole 2 full voltage test on October 14, 1992: (a) EDI, (b) EDV, and (c) THD.

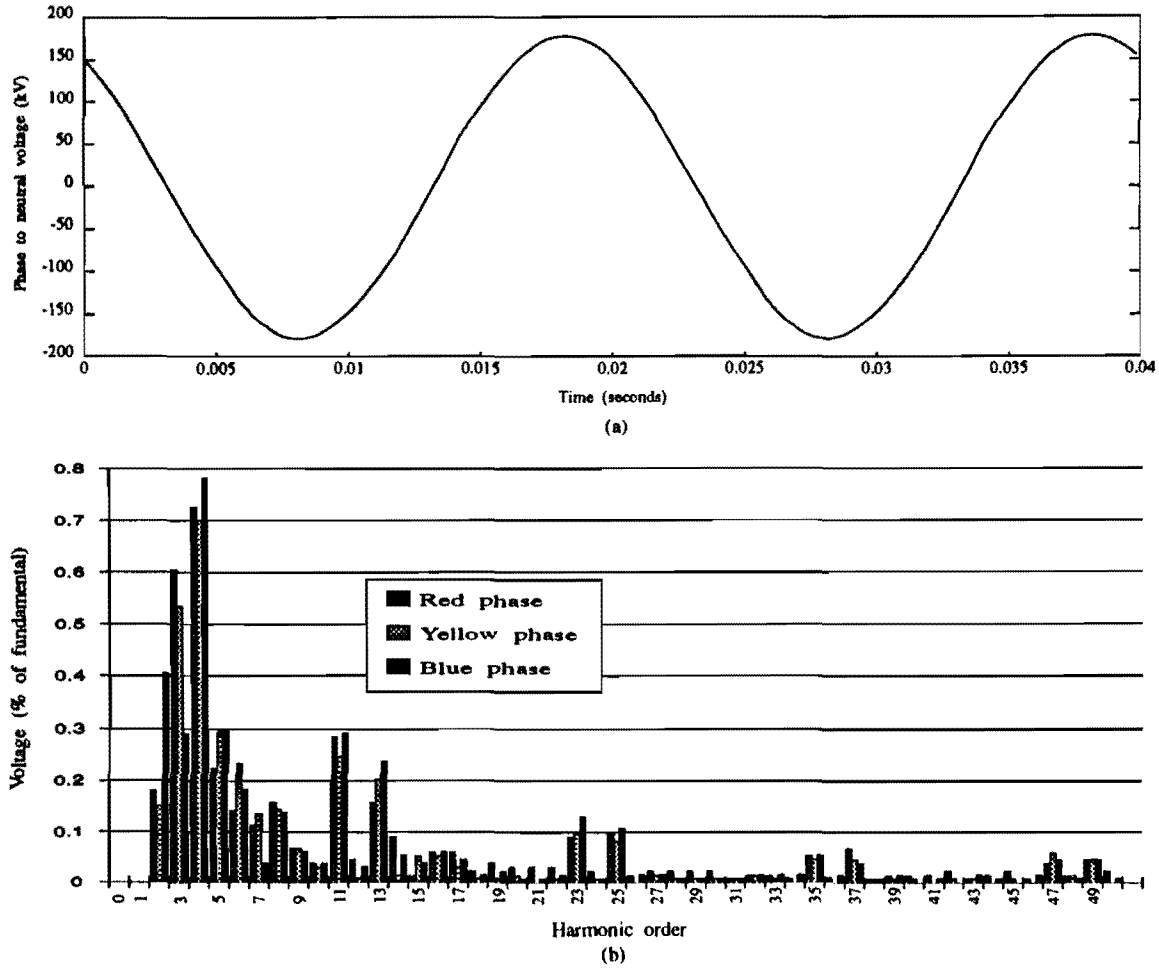

Figure 7.8 (a) Red phase voltage waveform, and (b) voltage harmonics corresponding to the maximum 4th harmonic voltage during the pole 2 full voltage test on October 14, 1992. The fundamental voltage in (b) has been suppressed.

The digital fibre optical link used in the CHART project proved invaluable in connecting CHART to the high voltage network. It completely removed the possibility of any ground loop and isolation problems, leading to very reliable results. The only problems experienced with this were the actual process of laying it out in the switch yard and rolling it back up onto barrels, which is time consuming, and the handling of its delicate ends and connectors, which were not rugged enough for field use. The use of laser beam links for data transmission from RDCMs has been mooted, although this would require an extensive error correction protocol to compensate for data loss if the beam happened to be interrupted. At present CHART uses a dual fibre cable, with one fibre used to transmit the sampling pulse from the DAPM to the RDCM, and the other to transmit converted digital samples from the RDCM to the DAPM. The use of a single fibre cable is currently being investigated. This would make the use of more expensive, but very rugged connectors more feasible, as well as decreasing the cost of the cable.

voltage dependent as well as frequency dependent. Consequently CVT tests must be performed at their full voltage (220 kV) for reliable results, which requires a high voltage harmonic source [Bradley *et al.*, 1985b].

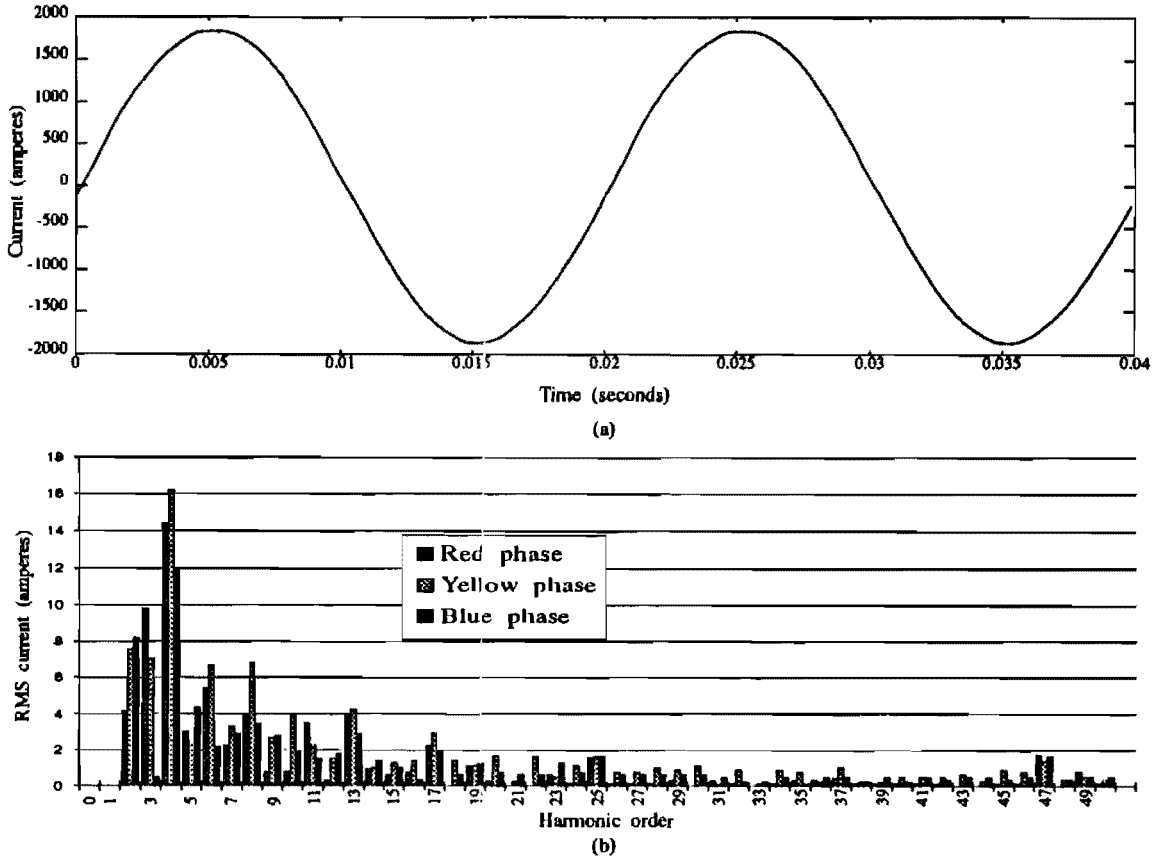

Figure 7.9 (a) Red phase current waveform and (b) current harmonics corresponding to the maximum 4th harmonic voltage during the pole 2 full voltage test on October 14, 1992. The fundamental current in (b) has been suppressed.

Although the amount of measured harmonic data was reduced by picking out the maxima in 10 second intervals, over the duration of the tests a large amount of data was stored (approximately 12 MB for 12 hours). Ways of dealing with this stored information have not yet been fully developed, and although the data was analyzed after the tests, the analysis should ideally be achieved on-line.

As well as providing Transpower New Zealand Limited with useful information regarding harmonic levels produced by the upgraded HVdc link, these tests have proven CHART II to be a very powerful harmonic monitoring instrument, and have shown that its results compare favourably with those collected by Design Power's harmonic monitoring equipment. Comparisons between the two systems were performed while monitoring rather than after, as Design Power's data was not available to us after the tests. CHART's remote data conversion modules and fibre optical links, parallel DSP data acquisition and processing system, and Windows based display system, essentially form a complete hardware and software system for harmonic monitoring of high voltage power systems. Any improvements on this, which were highlighted during the field tests, require only minor changes or refinements to the existing system. The data gathered during the tests is ideal material for a paper regarding harmonic measurement and harmonic data presentation, and it is intended to submit this paper for presentation at the IEEE Power Engineering Society Summer

Power Meeting in 1993, and for publication in the IEEE Power Engineering Society Transactions.

Chapter 8

CONCLUSIONS

The detrimental effects resulting from excessive harmonic levels on electrical power systems have prompted many countries to introduce standards limiting harmonic levels. As well as specifying limits for harmonic levels, these standards also set out requirements for harmonic monitoring instrumentation. This thesis has documented the design of a very sophisticated harmonic monitor for policing harmonic standards, known as the CHART II harmonic monitor. It is highly flexible allowing it to be easily adapted to meet the requirements of many standards, and furthermore, it has enormous potential as a research tool.

8.1 Features of the CHART II System

The main features of the monitor which distinguish it from other harmonic monitors are listed below.

- Remote data conversion modules convert CT or VT outputs to 16 bit digital signals, transmitted to the monitor by fibre optical cables. Conversion modules are sited remotely from the monitor, adjacent to CTs or VTs.

- Converting signals to digital signals at the source combined with the use of digital fibre optical cables isolates the monitor from hazardous high voltages in the switch yard, avoids ground loops in the instrumentation system, and stops induced noise from nearby conductors.

- Processing in the monitor is distributed amongst data acquisition channels with one DSP per data acquisition channel, and one micro-computer per two channels. This eliminates 'bottlenecks' caused by processing and bus bandwidth limitations.

- Additional channels can be easily added by inserting extra processing cards. The use of the Multibus II multiprocessing bus ensures that these extra cards can be automatically recognised and configured into the system. The only limitations on the number of channels is the power supply capacity and the number of free slots on the backplane. The theoretical maximum is 36 channels with a single backplane.

- The use of a synchronous sampling technique ensures that errors from the FFT are minimal.

- Special executable down-loading capabilities allow the development and use of many varied harmonic analysis techniques, ranging from averaging time domain data before FFT computation to taking the FFT over many cycles to resolve sub harmonics and inter harmonics.
- The use of multi-rate digital filtering techniques has simplified data acquisition hardware design and has lead to improvements in the acquired signals' SNR.
- A precision time referenced measurement capability is provided using a GPS satellite system, enabling simultaneous measurement at remote locations on a network.
- The use of a multitasking operating system running on a Multibus II 486 computer enables multiple tasks to collect data from each data acquisition and processing card and store it on a hard disk. It also enables tasks to collect data and distribute it to display workstations.
- Display workstations are networked on Ethernet, allowing more than one user to access CHART harmonic data using a standard PC running Microsoft windows with the CHART display software installed.

8.2 CHART Development History

Development of the first prototype of the CHART harmonic monitor began in 1986. It was designed to provide the type of information required by New Zealand legislation and was limited to only six channels. A prototype of this system was completed in 1990 and was subsequently used in a field trial at a New Zealand substation, which was reported in [Miller and Dewe, 1992a]. The prototype system was reported at the 4th ICHPS conference in [Lake *et al.*, 1990] and the 7th iRUG conference in [Miller *et al.*, 1990]. After the field trials and visits to the two conferences by Mr. M.B. Dewe and the author, a significant change to the first prototype was conceived, leading to the final prototype, CHART II, whose features are listed at the beginning of this chapter.

CHART II has enough processing power to continuously measure harmonic levels for many channels, meaning that there is no break in the acquisition and processing of source data, and its real-time capability provides the facility to observe the processed results as they occur. Its ability to precisely time stamp measurements made at remote sites on a network, extends its capabilities beyond harmonic analysis to fault location on ac and dc lines. A functional 10 channel prototype of CHART II was completed in September 1992, and was subsequently used in field trials in October and November of 1992. An overview of the CHART II system, covering design details such as its connection to the high voltage system, the parallel processing system and software used to compute harmonic levels, and the networked user interface to it was reported in [Miller and Dewe, 1992c]. The use of powerful DSPs in CHART II enabled the implementation of a multirate DSP technique for finding harmonics, leading to simplifications in data acquisition hardware, improved signal quality, and reduced computational requirements in the rest of the system. This technique is reported in [Miller and Dewe, 1992b], which includes a discussion covering the principles of filtering and sampling power system voltage and current signals for harmonic analysis.

8.3 Field Trials With CHART II

CHART II was used in field trials in October and November of 1992 at the Benmore terminal of the upgraded HVdc link. The harmonic monitoring system performed very well during these tests, and its display system proved invaluable for displaying harmonics throughout, as it was scaled to represent real quantities on the network. From these tests it became clear that it would be useful to display inter-harmonic signals as well as harmonics. This requires taking the FFT over more than one cycle, which can be achieved by modifying the DSP software. Sequence information regarding harmonics is also important, although this requires harmonic phase. To compute harmonic phase accurately, requires that the CT and VT frequency response characteristics be known. Although CHART II does find harmonic phase, phase results may have been distorted during the test due the unknown CT and VT responses. If these had been known, CHART could have compensated for them.

The field trials have proven CHART II to be a very powerful harmonic monitoring instrument, have shown that its results compare favourably with those collected by other harmonic monitoring instrumentation used during the field trials, and have provided Transpower N.Z. Ltd. with useful information regarding the harmonic performance of their upgraded HVdc link. As documented in the example of the 'Benmore pole 2 full voltage test' in Chapter 7, the test took some ten hours to complete. This is because the DC link power had to be held constant while harmonic measurements were taken, and then ramped up or down to the next power level for the next set of measurements. Each set of measurements took approximately 15 minutes using Transpower's HP 3565S system and Design Power's NOWA 1 system. The CHART system took 90 readings during each 15 minute interval, which indicates that the tests could have been performed in a much shorter time if CHART had been used on its own. This would have significantly reduced the cost of the tests, as the DC link would have been free for normal operation sooner.

8.4 Future Work With CHART

Required modifications to the CHART system as as result of the field trials are only minor, and do not involve a major system redesign. As mentioned above, a software addition to enable inter-harmonic signal detection would be useful. The main problem encountered during the field trials was with the fibre optical connectors which were not rugged enough for field use. Unfortunately rugged connectors are very expensive, although work is currently under way on a means of multiplexing the sampling signal to an RDCM and its return data onto a single fibre. This would halve the required number of connectors, enabling more rugged ones to be used.

To determine harmonic sequence information requires no change to CHART itself, as this already computes harmonic phase, and can compensate for non uniform magnitude and phase responses of CTs and VTs. Instead it involves using CHART to determine frequency responses of CTs and VTs used for harmonic measurements. It is planned to use the Electrical and Electronic Engineering Departments High Voltage Laboratory in conjunction with CHART to perform tests at 220 kV on VTs to determine the response characteristics of standard CVTs installed in switchyards

throughout the country. If the responses of these are known, it would be possible to compensate for them and thereby avoid the need to install special harmonic measurement CVTs for harmonic measurements. This seemingly straight forward experiment will be difficult to perform in practice, as it requires a high voltage harmonic source. This is because CVTs are voltage dependent as well as frequency dependent due to the effect of nonlinearities of the magnetic core on their output transformer [Bradley *et al.*, 1985b].

Although CHART was designed primarily for harmonic measurements, its has numerous other potential applications because it is essentially a data acquisition and processing system. It has the ability to make simultaneous time referenced measurements at remote locations on a network, which can allow the estimation of the state of the network at other locations. Using CHART, on-line decisions on changes of generation and loading on a network can also be made. An application of CHART that is under investigation is Expert Supervision of Convertor Operation in Real Time (ESCORT). This is the surveillance of the ac and dc side of an HVdc convertor for on-line control of its firing angle to minimize harmonic levels.

One of the key features of the CHART system is its processing capability enabling on-line monitoring of harmonic levels to reduce the data required for storage. However much effort is still required in this area, as the scope using CHART is very wide. A typical example of an on-line analysis method to be implemented is one that performs the following functions:

- Stores a 'snapshot' set of harmonic levels for each channel once every T minutes, where T is predefined. To ensure that harmonic levels can be compared between channels, they must correspond in time. Hence the particular cycle to store will be determined by the cycle number counter discussed in Section 5.2.2.3. The reason for storing this snapshot is to give an indication of background harmonic levels.

- Every harmonic for each channel is monitored, and if any one changes by a certain amount, a number of cycles prior to and following the change are stored. All channels are instructed to store the same cycles if this occurs.

- Every harmonic for each channel is monitored, and if any one exceeds a threshold of a limit (obtained from standards), a number of cycles prior to, during, and after the event are stored. All channels are instructed to store the same cycles in this event.

Work on an antenna for detecting fault wave fronts on a dc transmission line, and work on the CHART real time clock, is almost complete. This will extend CHARTs functions from harmonic monitoring to fault location monitoring of HVdc lines [Dewe *et al.*, 1992].

Chapter 9

EPILOGUE

In the intervening time between submitting this thesis in December 1992 and receiving the examiners' reports in February 1993, the networking software for the CHART II 486/133SE computer arrived. As discussed in Chapter 5, the production of this software was delayed, meaning that the Ethernet link between the PC workstations and the 486/133SE Multibus II computer could not be commissioned. The networking software has now been successfully installed and configured into the iRMXIII.1.3 operating system running on the 486 computer. Standard packages such as FTP (File Transfer Protocol) and TELNET (a network terminal emulator) are now available on the CHART II Multibus II system, opening it up to the other networked computing facilities. The Ethernet link software to the workstation PCs has also been written using this networking software, and has lead to an enormous improvement in the CHART II instruments user interface and display capabilities.

There remains a lot of work to be done in rigorously evaluating the systems performance. Work on this has already begun by measuring the performance of the ADCs in the data acquisition stages of CHART. Once a reliable measurement scheme is devised, their performance will be optimized. The numerical errors introduced during harmonic computation by the fixed point DSPs must be analyzed. This will give an indication of the lowest possible harmonic levels that can be measured in the presence of the fundamental component.

On-going development of the CHART instrument is likely to involve moving the DSPs and their host processors out into the RDCMs. This would demand higher power supply ratings from each RDCM, although as the bulk of an RDCM is power supply, this should not present a major problem. The advantage in doing this is it eliminates the need for the expensive DAPMs with Multibus II interfaces. These would be replaced by one Multibus II processor card developed to collect data from all RDCMs. The complete system may even be moved to a PC platform, eliminating the need for Multibus II all together. Obvious problems with moving the DSPs out to the RDCMs are: the control of the DSPs, executable down-loading to them, and time stamping of their processed data. Nevertheless the advantages of the new architecture provide the motivation for solving these problems. A move to floating point DSPs should also be considered given the hardware experience gained from the CHART II exercise.

Appendix A

COLLECTED PAPERS ON THE CHART SYSTEM.

This appendix contains copies of all papers and reports written regarding the CHART system. The most recent papers are listed first.

Appendix A.1 was written in January 1993 for presentation at the 1993 IEEE Power Engineering Society (PES) Summer Power Meeting, and for publication in the PES Transactions. Unfortunately the usual deadline of the end of January 1993 for this meeting was brought forward, without the Author's knowledge, to the end of December 1992. The paper has now been submitted for presentation at the 1994 PES Winter Power Meeting, and for publication in the IEEE Transactions. This appendix relates to Chapter 7 of this Thesis.

Appendix A.2 relates to Chapter 6 of this thesis and was written during January and February of 1992. It was presented by Mr. M.B. Dewe at the September 1992 ICHPS V conference in Atlanta, USA, and has been refereed and accepted for publication in the IEEE Transactions.

Appendices A.3 and A.5 relate to Chapter 5. Appendix A.3 was presented at the July 1992 PES Summer Power Meeting in Seattle, USA, and has been refereed and accepted for publication in the IEEE transactions. Appendix A.5 was written in August 1991, and was presented by Mr. M.B. Dewe at the February 1992 PES Winter Power Meeting in New York, USA. It has been refereed and published in the October 1992 IEEE Transactions on Power Delivery.

Appendices A.4 and A.7 relate to Chapter 4 of this thesis. Appendix A.7 was written during July and August of 1990 after the July 1990 Field trials with the CHART I system at the Islington Substation. These tests were performed in conjunction with Neil McKenzie of Design Power New Zealand. The report highlights some of the practicle issues and limitations involved in making measurements with the CHART I system. Appendix A.4 was written during September 1991 and was published in the proceedings of the Annual Conference of the Institute of Professional Engineers New Zealand (IPENZ), September, 1992, in Christshurch, New Zealand. It was Presented by the Author.

Appendices A.6, A.8, A.9, and A.10 relate to Chapter 3 of this thesis. Appendix A.6 was written during June of 1990 and won the award of an 'all expenses paid' trip for the presenter to the September 1990 iRUG conference in St. Louis, Missouri, USA. It was presented by the author and has been published in the proceedings of the 1990 iRUG conference. Appendix A.8 was written during January and February of 1990 for publication in the proceedings of the October 1990 ICHPS IV conference, in Budapest, Hungary. It was presented by Mr. M.B. Dewe. Appendices A.9 and A.10 were written during May 1989 and were published in the proceedings

of the 26th National Electronics Conference (NELCON), in Wellington, September 1989. They were presented by their respective authors.

A.1 Harmonic Measurements made on the NZ HVdc Link

HARMONIC MEASUREMENTS MADE ON THE UPGRADED NEW ZEALAND INTER-ISLAND HVDC TRANSMISSION SYSTEM

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Member

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Senior Member

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Abstract - This paper introduces the recent upgrade to the New Zealand inter-island HVdc transmission system. It then details the procedure of one of several tests conducted to measure harmonic levels created by the upgraded transmission system. Harmonic levels were measured using the CHART (Continuous Harmonic Analysis in Real-Time) harmonic monitoring instrumentation. The connection of CHART to the high voltage network and its configuration during the test is discussed. A sample of results gathered while monitoring are presented, including characteristic harmonics of the converter, and maximum voltage and current levels up to the 50th harmonic for each of the three a.c. phases. During the tests one of the two a.c. harmonic filters was switched out to observe its effect on harmonic levels. It was found that with both a.c. harmonic filters operating, most harmonic levels were lower than with only one filter operating. However some harmonic levels, namely the 4th harmonic, were larger with both filters operating. The paper is concluded with a discussion of the results and of the difficulties encountered in measuring harmonics of very low level.

INTRODUCTION

The New Zealand inter-island HVdc transmission system reported in [1] and shown in Figure 1 has recently been upgraded from 600 MW to 1240 MW. The upgrade involved connecting the existing two poles in parallel to form one 12 pulse pole and adding a new 12 pulse thyristor converter pole with its associated converter transformer and a.c. harmonic filters. The upgraded configuration at the Benmore terminal of the HVdc link is illustrated in Figure 2.

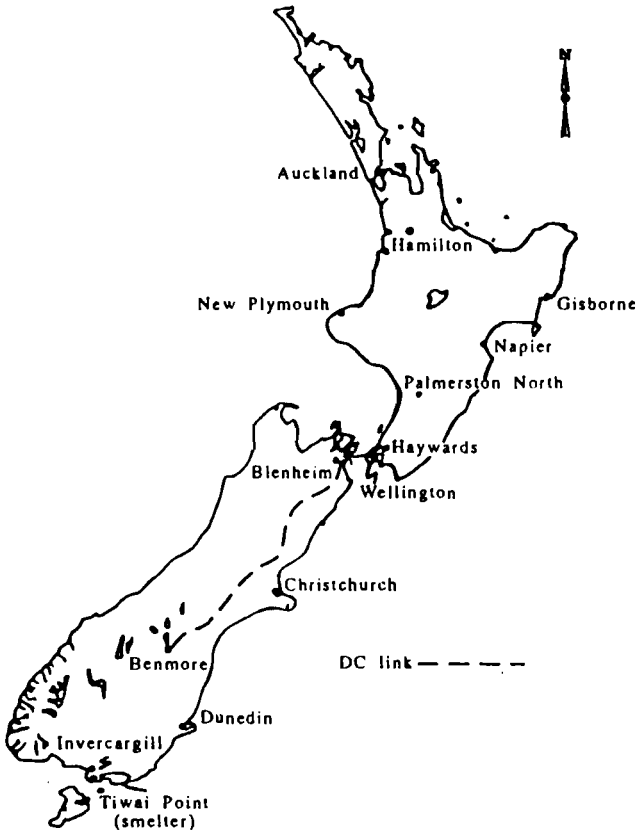

Figure 1: The New Zealand (NZ) inter-island HVdc transmission system between Benmore and Haywards.

As part of the commissioning tests on the upgraded HVdc link, the harmonics generated by it and fed back into the a.c. system were required to be measured to verify the effectiveness of the new a.c. harmonic filters. The new pole has two identical a.c. harmonic filters, each having one section tuned to the 11th and 13th harmonics, and a high pass at the 24th harmonic. A number of tests were carried out at each end of the link, including operating only the new pole (pole 2) at both full and reduced voltage, and bipole tests. This paper discusses a test made on the new pole operating at its full voltage, and measurements made at the Benmore end of the link.

A prototype unit of the CHART (Continuous Har-

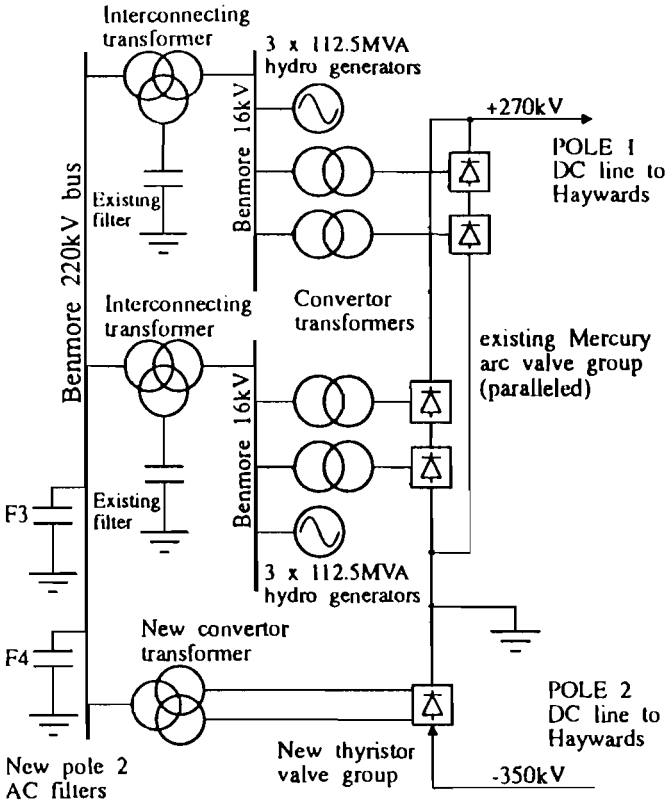

Figure 2: The Benmore terminal of the upgraded HVdc transmission system.

monic Analysis in Real-Time) system described in [2] was used to measure harmonic levels throughout the tests together with Design Power New Zealand's harmonic monitoring instrumentation. Design Power New Zealand (DPNZ) is a subsidiary of the New Zealand Electricity Corporation (ECNZ) and offers a consulting service to other ECNZ subsidiaries - in this case Transpower New Zealand (TPNZ) who manage the New Zealand national grid. DPNZ's instrumentation comprises three NOWA 1 harmonic monitors connected to a PC. TPNZ contracted DPNZ to make the measurements and requested that measurements also be made using a prototype of the CHART system as an exercise in proving CHARTs ability as a monitor. The parameters required by Transpower from the tests were Total Harmonic Distortion (THD) and individual harmonic magnitudes for both current and voltage.

The procedure of the test carried out is discussed, including the connection of CHART to the High Voltage (HV) network, and CHARTs configuration throughout the test. A number of results from CHART are then presented giving an indication of what results CHART can provide, and of the harmonic performance of the converter under various operating conditions, followed by a discussion of the results and of the test. The paper is concluded by pointing out the achievements of the tests and the difficulties involved in making harmonic measurements.

PROCEDURE

The Harmonic Test on the New Converter

The purpose of this test was to examine the effectiveness of the a.c. harmonic filters at various loads transferred on the dc transmission system with only the new pole operating and the ground used as a return path for dc current. The converter operating as a rectifier was ramped from minimum power to full power and back down in stages as shown in Figure 3, with one of the two filter banks switched out at full power to observe its effect.

The test procedure was dictated by DPNZ and was based on the capabilities of their equipment. Their main requirement was that at each stage in the test the power level be held constant for at least 15 minutes. This was to allow their instrumentation to make a sufficient number of readings at each power level. In addition to this they required the tests to be extended when 350 MW was reached during ramping up to enable them to decrease the Current Transformer (CT) burden resistors discussed in the next section, and to increase them when ramping down. The reason for doing this was to avoid saturating the analog input of their equipment.

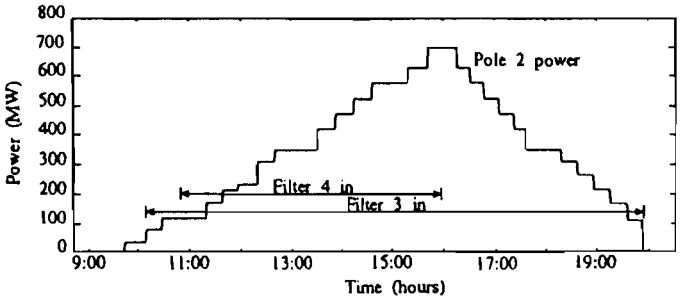

Figure 3: Pole 2 power profile for the test.

Harmonic currents injected into the 220 kV system at Benmore by the new pole of the converter were found by connecting harmonic monitoring instrumentation to CT418 of Figure 4. The connection of CHART to these transducers is discussed in the following section.

Throughout this test, pole 1 and its harmonic filters were left off to minimize background harmonic levels.

CHARTs Connection to the HV Network

The instrumentation windings of conventional metering CTs, which are part of existing installed equipment, were used to measure the current in each phase flowing into the converter. The secondary windings of these transformers were terminated in 15 Ω burden resistors, which are part of DPNZ's harmonic monitoring equipment, as illustrated in Figure 5(a).

CHART Remote data conversion modules were used to convert the voltage across the resistor illustrated in Figure 5(a) to digital samples which were transmitted to the CHART parallel processing unit by fibre optic cables, discussed in [2].

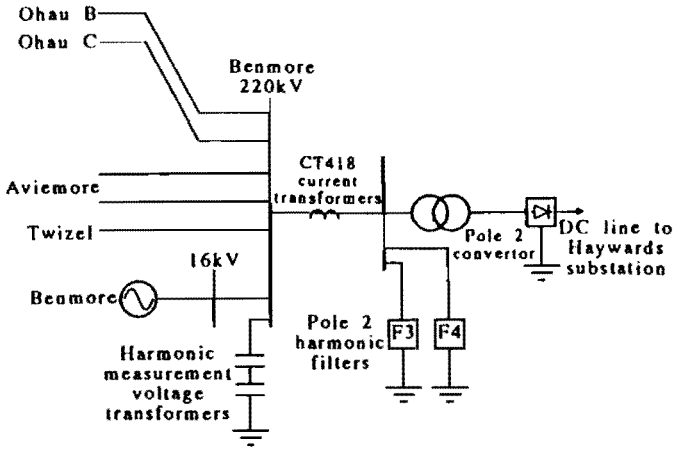

Figure 4: Current and voltage transformer locations for the harmonic test.

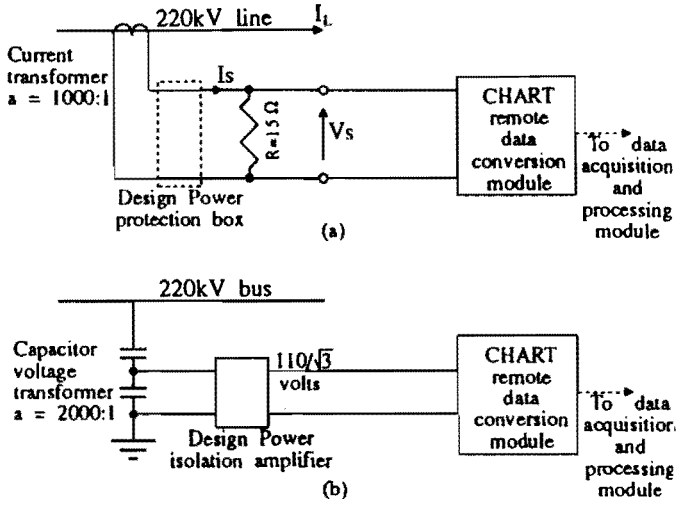

Figure 5: The connection of CHART to the high voltage network. (a) Current measurement. (b) Voltage measurement.

Although the CHART instrument has the ability to compensate for non uniform CT magnitude and phase frequency responses, no compensation for computed harmonic currents was made, as no data regarding the CTs used was available. The assumption that the CT frequency response is uniform is however valid for all frequencies below 5KHz [3].

Measurement of the 220 kV bus harmonic voltage using conventional VTs is highly inaccurate, as these have resonant points in the frequency range of interest [3]. Although research into the determination of VT frequency response characteristics has been carried out [4], no complete data of VT responses was available, making it impossible to compensate computed harmonic voltages for the transducer characteristics. TPNZ own a set of three harmonic measurement Capacitor VTs (CVTs) for use in harmonic voltage measurements of 220 kV and 110 kV three phase power systems. These have uniform magnitude frequency responses in the harmonic analysis band up to the 50th harmonic, and were installed on the 220 kV bus especially for the tests. CHART was connected to these as shown in Figure 5(b). The harmonic measurement CVTs have a 2000:1 ratio, giving a nominal output of 110Vrms phase-to-phase from the 220 kV bus bar.

The Configuration of CHART

To monitor 3 phase current and voltage, 3 two channel processing modules (DAPMs, discussed in [2]) were used, with each DAPM used to monitor one voltage channel and one current channel.

Processing of acquired data is discussed in [5], and essentially consists of a digital antialiasing filter followed by a Fast Fourier Transform (FFT) to find the Discrete Fourier Transform (DFT) of the sampled data. The sampling rate and FFT record length were arranged so that the FFT output corresponded to the fundamental and harmonics of this. The FFT output was transformed from complex Cartesian form to polar coordinates, giving the magnitude and phase of each harmonic.

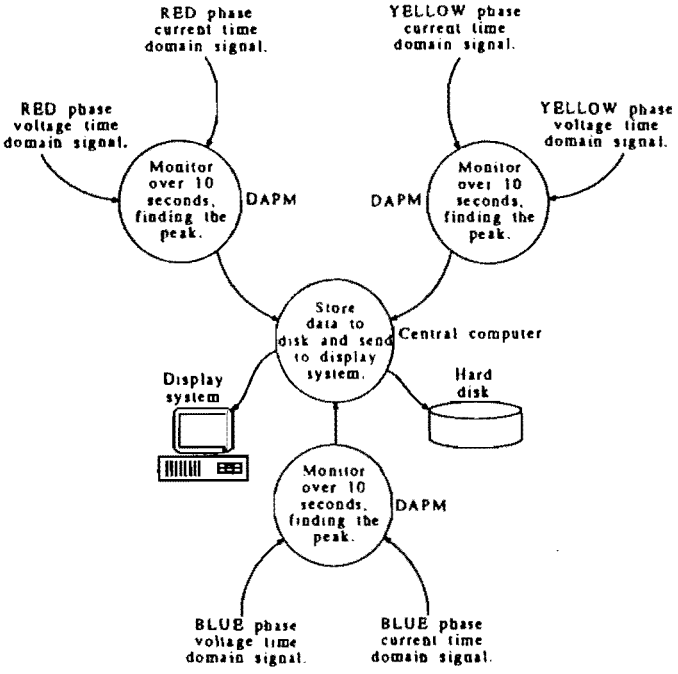

Figure 6: Data flow and processing performed during the harmonic tests.

Each DAPM was configured to monitor the fundamental component of its current channel over a period of 10 seconds. At the peak fundamental current in this interval, harmonics of both current and voltage were stored, along with the original time domain signals. This data was then forwarded to a central computer where it was time stamped and stored. Current was monitored instead of voltage, as it varies continuously over a wide range, whereas voltage varies only slightly. Data flow and processing in the system for the harmonic tests is illustrated in Figure 6. It should be noted that the CHART system can be configured to any desired monitoring/storage algorithms. The particular configuration used here was chosen to suit the test procedure which required a number of readings to be taken at each power level.

A display workstation was connected to the central computer during the tests to enable the display of harmonic levels and time domain signals for each channel.

RESULTS

Figures 7 and 8 show a sample of RED phase voltage and current harmonics measured during the test. The fundamental current is shown to enable a comparison between it and the current harmonic levels, and the points at which the CT resistors were changed are marked, together with filter switchings. All voltages are shown as a percentage of the fundamental voltage. Figures 9 and 10 illustrate the maximum voltage and current harmonic levels recorded during the test for all three phases up to the 50th harmonic.

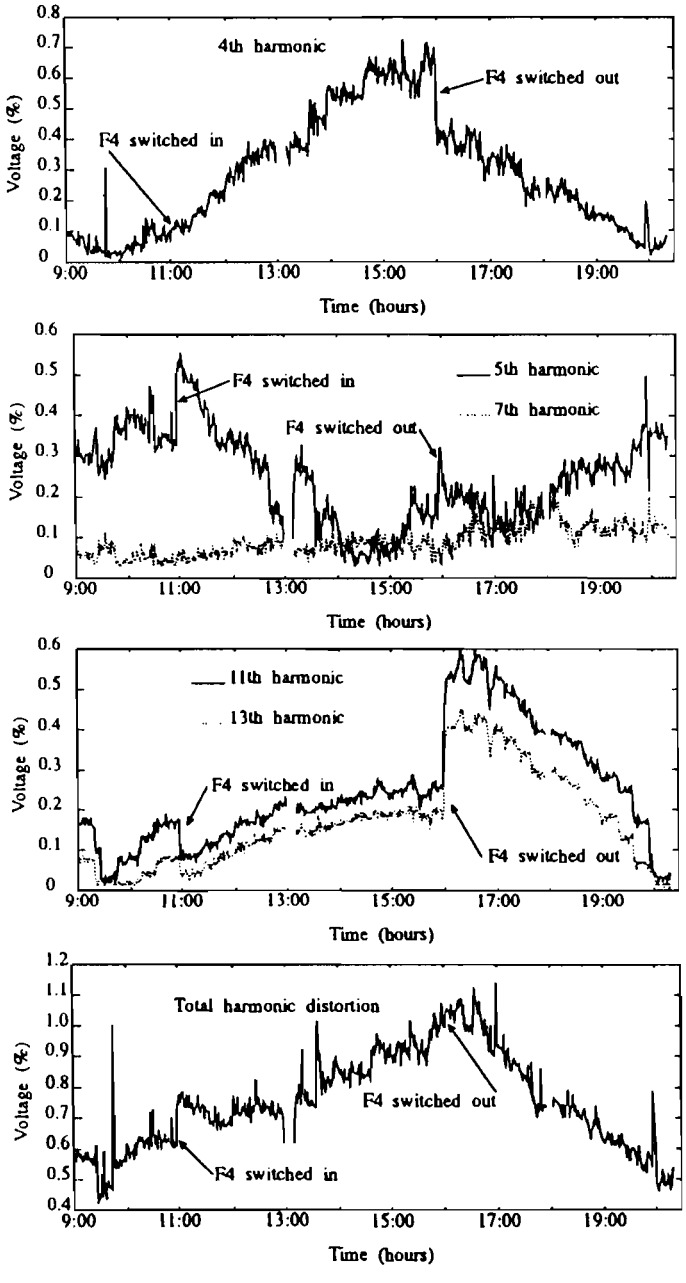

Figure 7: Red phase voltage harmonics, October 14, 1992.

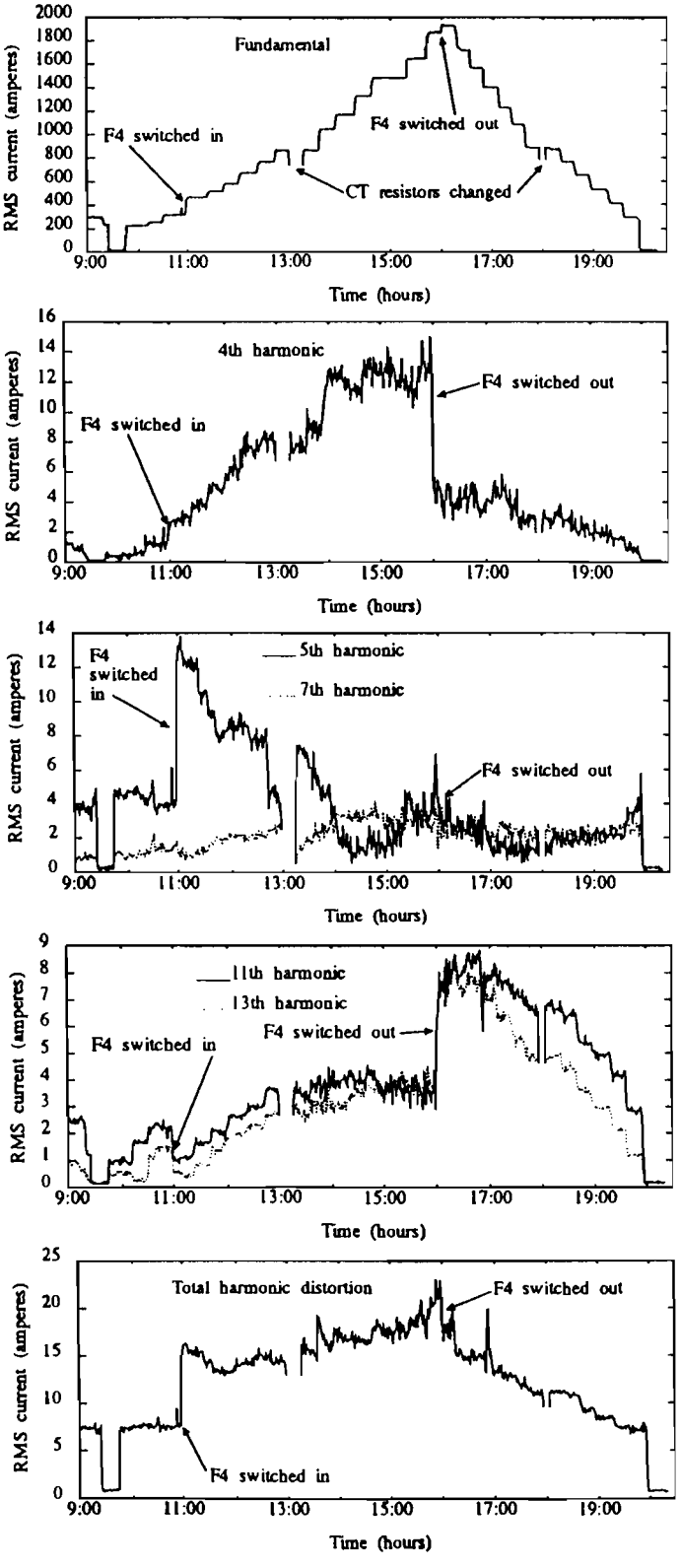

Figure 8: Red phase current harmonics, October 14, 1992.

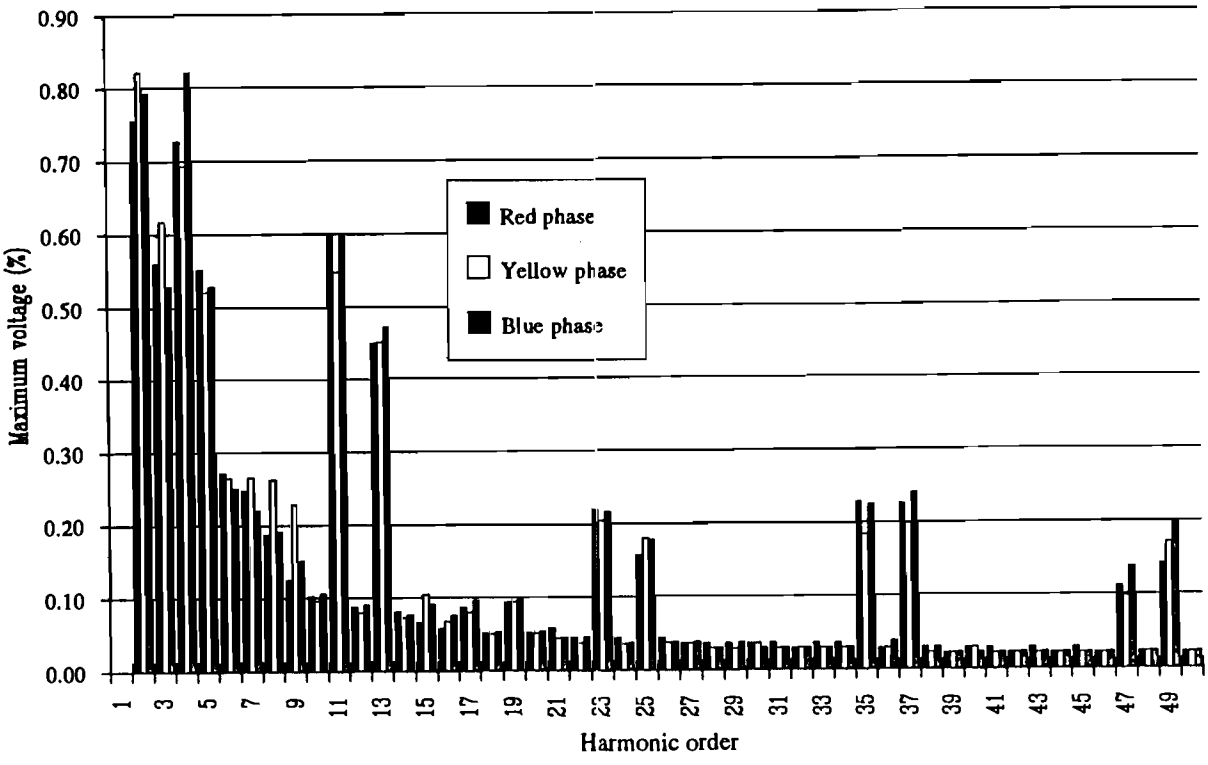

Figure 9: Maximum voltage harmonic levels recorded throughout the test.

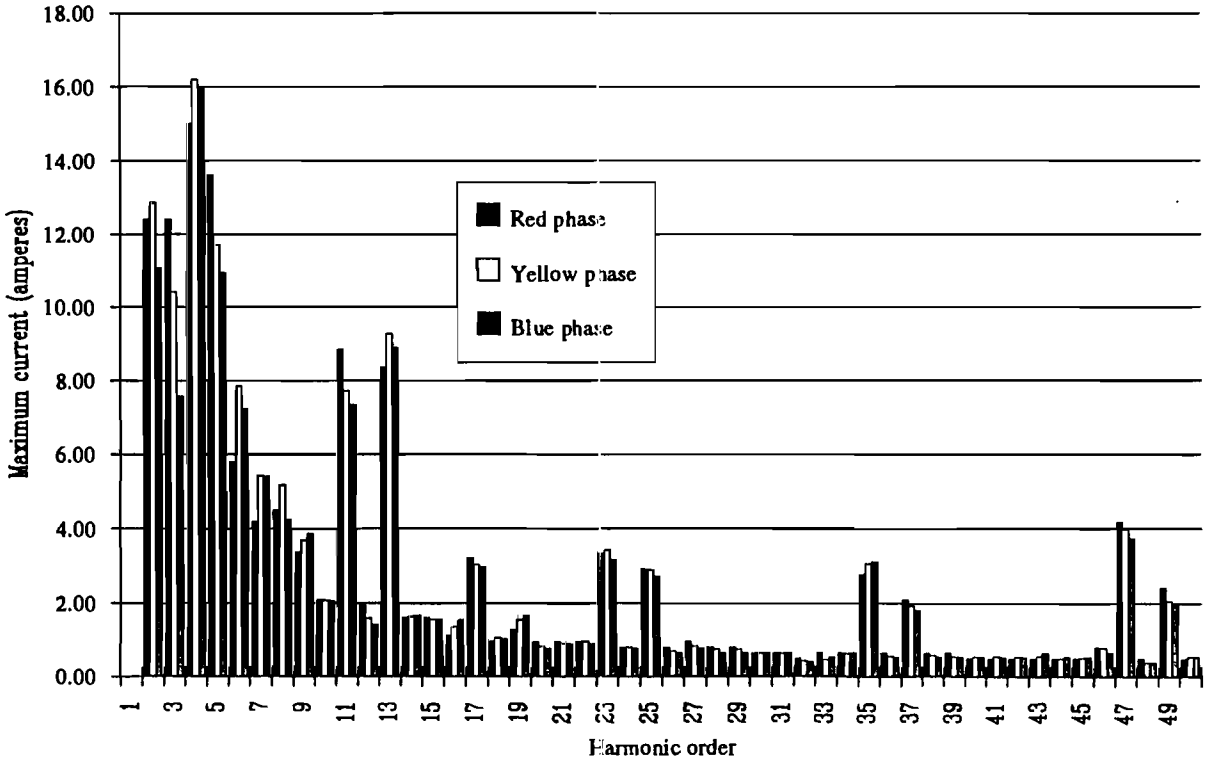

Figure 10: Maximum current harmonic levels recorded throughout the test.

DISCUSSION

Discussion of Results

With reference to the results of Figures 7 and 8, the following comments are made:

1. The figures show that the 11th and 13th harmonics for both voltage and current are lower with the second harmonic filter bank, F4, switched in. This is to be expected, as the filter banks are tuned to these two harmonics.

2. While the CT resistors were changed, the harmonic levels decreased. This is because the converter was stopped to change the resistors, which in turn ensured a minimal current flow through the line monitored by CT418 - a safety precaution in case the CT was accidentally open circuited while changing the resistors.

3. The 4th harmonic is shown to illustrate that it is higher when the second harmonic filter, F4, is switched in. This is an indication of a possible harmonic resonance which moves to the 4th harmonic when the second filter is switched in. The existence of the 4th harmonic indicates an asymmetry between phases in the firing of the thyristors.

Unfortunately it was not possible to make background readings of current harmonic levels before and after the test. The connection to the CTs was controlled by DPNZ who only allowed the connection of their burden resistors during the test. The whole manner in which the tests were carried out was dictated by the requirements of DPNZs harmonic monitoring equipment. From the viewpoint of the CHART system and TPNZ, the tests were basically a 'proving' exercise.

Difficulties Encountered

The DPNZ requirement to change the CT resistors twice during the test was considered an impediment to the test flow. As pointed out previously and illustrated in Figures 7 and 8, the converter had to be stopped to allow this, causing a discrepancy in harmonic levels before and after the change. The CHART instrument does not require this change as it is set up to match the CT, its burden resistor, and maximum expected line current before monitoring, thereby avoiding interruption during a test.

Accurate monitoring of harmonic voltage and current is a difficult task requiring precise data acquisition in an electrically noisy environment. The CHART instrument overcomes this difficulty by converting analog signals to digital almost at their source (next to the CTs and VTs) by independent battery powered converter modules (RDCMs), connected to the CHART processing system by fibre optic links. The actual connection to CTs and VTs is controlled by TPNZ who will only allow approved equipment to be directly connected, to avoid for instance the accidental open circuiting of a CT. It was therefore necessary to connect the CHART instrument to the output of approved DPNZ signal conditioning equipment, which was another possible source of noise to the CHART system.

CHART uses 16 bit Analog to Digital converters (ADCs) to minimize quantization noise produced during analog to digital conversion. The full advantage of this is only obtained if the analog signals to be acquired have the full dynamic range of the ADC input. This was simple enough to arrange for voltage which only varies slightly about a nominal value. However for the duration of the test current was varied over the full dynamic range of the ADCs, meaning that the low level signals were significantly affected by external noise sources such as electromagnetic induction in leads from transducers, quantization noise, and round off errors from finite precision arithmetic.

When harmonic levels are significantly lower than the fundamental component, as in the case of this test where they were less than 1% of the fundamental's level, it is important to maximize the dynamic range of the ADC. As explained previously, this is impossible to achieve for current signals throughout the normal range of operating conditions. It is therefore essential that the ADCs be very high quality, having a very good signal to noise ratio and that the connection to CTs be carefully shielded, and ideally as direct as possible. Sources of noise in harmonics are set out below:

- Electromagnetically and Electrostatically induced noise.
- Quantization during analog to digital conversion.
- Round off errors from finite precision arithmetic.
- Non uniform frequency responses of CTs and VTs used to measure line current and bus voltage.
- Spectral leakage from the FFT.
- Aliasing errors introduced by sampling.

It was anticipated that harmonic phase would be able to be used to compute such quantities such as harmonic impedance and power, and to find the sequences of harmonics by comparing phase between the three phases of the power system. Although possible in principle, this is difficult to achieve in practice due to significant phase distortion as a result of very low level harmonics amongst noise in the current signals. This phase distortion is at present under investigation. If current had been measured between the converter and its a.c. filters (shown in Figure 4), harmonic current magnitudes would have been higher, facilitating more accurate measurements of phase. The purpose of the tests was however to examine the effectiveness of the a.c. filters, and the point of connection for harmonic monitoring instrumentation was dictated by TPNZ requirements, together with the permission to connect to their equipment.

CONCLUSION

The primary purpose of this test has been to provide Transpower NZ with information relating to the performance of the a.c. harmonic filters on the new pole of the Benmore terminal of their HVdc transmission system. It has also been beneficial as an exercise in which to test a prototype of the CHART system in a real situation. The test proved very demanding, requiring accurate measurement of current signals varying in amplitude over a wide range (from very low levels to high levels). The signals were acquired from transducers located in the very noisy environment of an HV switchyard. As a result of this test it was found that measurement of harmonic phase angle of low level signals is not straight forward in a real situation. Error in harmonic phase angle measurement is currently under investigation.

To reduce errors introduced during data acquisition, care must be taken to maximize the dynamic range of ADCs. This is not possible for current which, as in this test, may vary over a wide range. In this case it is important to use high quality ADCs with high signal to noise ratios and to take care in running leads in the switch yard. Ideally tests should avoid reducing currents to such low levels, as the harmonic quantities that are being measured are generally at low levels to begin with.

Future measurements made with CHART will be made by connecting to transducers closer to the converter, where harmonic currents will be larger, with more emphasis on harmonic phase, as well as using CHARTs precise time stamping ability to make measurements at remote locations on a network and enable their comparison. Fault location on a network will also be investigated.

ACKNOWLEDGEMENT

The authors thank Transpower NZ Ltd. for allowing them to make harmonic measurements during the commissioning of the upgraded NZ HVdc transmission system, and Dr. C.S. Kumble of Transpower NZ Ltd. for arranging the tests with CHART. They also thank Mr. N. McKenzie of Design Power NZ Ltd. for his assistance during the tests, and Mr. B. Ireland of Transpower NZ Ltd. for coordinating the tests. The authors acknowledge the financial assistance of Transpower NZ Ltd., and thank the members of the Power Systems group of the Department of Electrical and Electronic Engineering for their advice and assistance, including Mr. Chen Shuin, Mr. D. Chuah, and Mr. V. Kuhlmann. In particular the authors thank Mr. D. Sallis of the Department of Electrical and Electronic Engineering for his invaluable assistance during the tests.

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A.2 Multi-rate DSP Techniques used in Harmonic Measurement

The Application of Multi-rate Digital Signal Processing Techniques to the Measurement of Power System Harmonic Levels

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Abstract - The concepts of filtering and sampling power system voltage and current signals for harmonic analysis using the fast Fourier transform (FFT) algorithm are introduced. The application of a multi-rate digital signal processing technique for harmonic analysis is then discussed and the design of a polyphase decimation finite impulse response (FIR) filter, for use as an anti-aliasing filter in oversampling applications, is covered. The implementation of this filter in conjunction with an FFT by a digital signal processor is described, and results of timing tests on the algorithms are presented. The instrument used to implement these techniques is CHART - an advanced data acquisition and parallel processing system aimed specifically at continuous real-time power system signal monitoring.

INTRODUCTION

The CHART project is concerned with finding the harmonic levels of as many as 32 power system voltage or current signals on a cycle-by-cycle basis continually in real-time. Hence the acronym CHART - Continuous Harmonic Analysis in Real-Time [1].

Traditionally the CHART harmonic monitor has sampled voltage and current signals at the lowest rate possible to resolve up to the 50th harmonic. This has the advantage that the system does not have to cope with much data, as it is at a low rate. It also enables slower and therefore relatively inexpensive analog to digital convertors (ADCs) to be used for data acquisition. However harmonic levels are computed using the fast Fourier transform (FFT) to find the discrete Fourier transform (DFT), which can be efficiently implemented using digital signal processors (DSPs).

In order to increase the number of channels of the CHART system to greater than 30, a two channel Multibus II based DSP board was developed [1]. A typical system consists of four or more of these boards, which can be easily added to increase a systems potential by adding processing capability at the same time as extra channels. An additional advantage of using DSPs is that many different harmonic analysis algorithms can be tested, as the system is designed to allow simple loading of executables into a DSPs program RAM [1]. This paper describes a multirate DSP technique implemented using CHARTs DSPs to measure voltage and current harmonic levels. The approach taken is to oversample power system signals, thereby reducing the complexity of front end anti-aliasing filters. This was made possible with the advent of faster ADCs - a spin off from digital audio research. The more stringent anti-aliasing filter required before the FFT is realized by the DSPs in the form of a finite impulse response (FIR) filter. The output from this filter is decimated to reduce the sampling rate for the FFT, which is also implemented by the DSP. This technique was used as it made full use of the processing capability offered by the DSPs leading to a significant reduction in data acquisition hardware complexity.

The paper begins by introducing some important sampling concepts and discusses sampling for the FFT. It then describes the multirate DSP technique employed by CHART, including the anti-aliasing FIR filter design and its structural manipulation for computational efficiency. It concludes by discussing the FFT implementation, data flow through the system, and results of timing tests on the various algorithms implemented on the DSPs.

DATA ACQUISITION

The approach adopted in the determination of voltage and current harmonic levels using the CHART instrument is one of digital signal processing. This requires that voltage and current waveforms be represented by a set of digital samples of discrete magnitudes, taken at discrete instants in time. The *sampling* process is accomplished by multiplying the volt-

age or current waveform, represented by $h(t)$ in figure 1(a), by the sampling function $\delta_0(t)$, illustrated in figure 1(b). This results in a signal

$$\hat{h}(t) = \sum_{k=-\infty}^{\infty} h(kT)\delta(t - kT) \quad (1)$$

which is a set of uniformly spaced samples, T seconds apart, illustrated in figure 1(c). The sampling period is defined as T and the sampling rate as

$$f_s = \frac{1}{T} \quad (2)$$

For a unique correspondence between the continuous function $h(t)$ and its samples $\hat{h}(t)$, the sampling period T must be chosen to satisfy the requirements of the Nyquist sampling theorem [2] which essentially states that the signal $h(t)$ must be band-limited to f_a and that

$$f_s > 2f_a \quad (3)$$

This is illustrated in figure 1(c) which depicts the Fourier transform of the sampled signal. If this condition is not met, the spectrum centred at f_s will interfere with that at 0, distorting the sampled signal, an effect known as *aliasing*.

In practice it is impossible to completely band-limit a signal, a problem circumvented by low pass filtering the signal before sampling, and sampling at such a rate that aliasing is negligible. The level below which aliasing is negligible is the signal noise floor, determined predominantly by quantization noise, discussed in the following section.

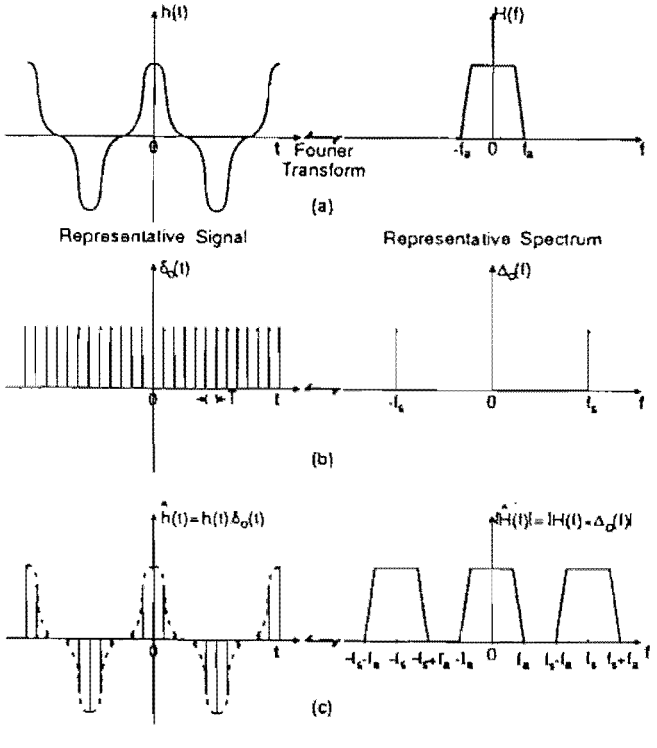

Figure 1: Sampling of a signal.

Signal Quantization

The sampled signal must be quantized to a number of discrete magnitudes for it to be represented by a finite word length machine. Quantization is usually performed during analog to digital conversion, and creates a quantization noise voltage. The approximate theoretical RMS signal to quantization noise ratio of an N-bit ADC for a full-scale sinewave input is given by [3]

$$SNR(dB) = 6.02N + 1.76. \quad (4)$$

This provides a noise level below which aliasing is negligible, as the aliased signal will not be resolved by the convertor, giving an indication of the filter response required to avoid noticable aliasing.

This filter response is depicted in figure 2, with the aliased response shown dotted about f_s. The filter has a roll-off from the cut-off frequency f_c to f_a which is sufficiently steep to ensure an attenuation of A dB at f_a when $f_s = 2f_a$. This assumes that the signal being sampled may contain frequency components of full power beyond the cut-off frequency. Such a stringent filter may not be required for real signals.

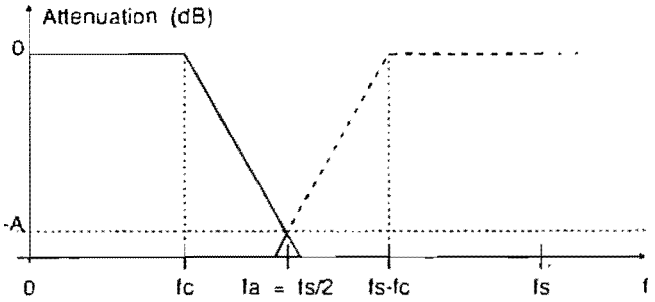

Figure 2: Anti-aliasing filter response.

It is an approximation to apply equation 4 to the signals measured on a power system which may be distorted from an ideal sinewave. It does however give an indication of the attenuation required to avoid aliasing and this equation has been used in this application.

Sampling for the FFT

The sampled signal $\hat{h}(t)$ of equation 1 must be truncated to a finite number of samples for machine computation. This is achieved by multiplying the sampling signal illustrated in figure 3(a) by the rectangular truncation function of figure 3(b) to yield the finite sequence of N samples illustrated in figure 3(c).

A sinewave is used to illustrate this process in both the time and frequency domains.

The Fourier transform of the rectangular truncation function is the $sinf//f$ function, also illustrated in figure 3(b). The Fourier transform of the sampled truncated signal of figure 3(c) is obtained by convolving the sampled signals Fourier transform with the $sinf//f$ function of figure 3(b). If the periodic signal $h(t)$ is represented by a Fourier series expansion and is band limited to N harmonics, the sampled truncated signals Fourier transform becomes

$$H'(f) = T_0 f_s \sum_{n=0}^{N} \alpha_n \frac{sin(\pi T_0[f - nf_0])}{\pi T_0[f - nf_0]} \qquad (5)$$

where α_n are the complex coefficients of the Fourier series, and f_0 is the fundamental frequency of the periodic signal $h(t)$. The derivation of this is given in appendix A. Figure 4(a) depicts $H'(f)$, which is essentially the summation of $sinf/f$ functions centred on each harmonic frequency. The width of the $sinf//f$ functions is dependent on the truncation interval width of figure 3(b). If the truncation interval is equal to an integer multiple of the period of $h(t)$ (that is $T_0 = n/f_0$, where n is an integer) the $sinf//f$ function centred on each harmonic will be maximum at the harmonic frequency and zero at all adjacent harmonics.

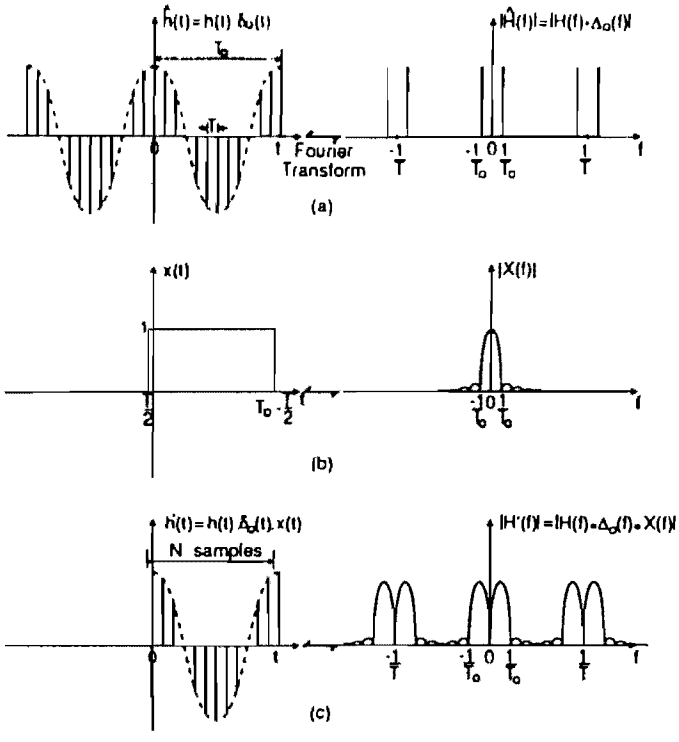

Figure 3: Truncation of a periodic signal and the resultant Fourier transform.

When the truncation interval is not equal to an integer multiple of the fundamental period ($T_0 f_0 \neq n$, where n is an integer), then the $sinf//f$ function at each harmonic will interfere with adjacent harmonics - an effect known as *spectral leakage* [4]. The interference of an harmonic adjacent to another is given by

$$A(dB) = 20log_{10}|\frac{sin(\pi T_0 f_0)}{\pi T_0 f_0}|. \qquad (6)$$

where f_0 is the fundamental frequency and T_0 is the truncation interval length. The derivation of this equation is given in Appendix B.

If a voltage or current signal is sampled at a constant frequency f_s such that the truncation interval corresponds to exactly one period of the 50Hz or 60Hz fundamental frequency, no interference from adjacent harmonics will occur. However, fluctuations in the fundamental frequency will effectively change the truncation interval, causing spectral leakage. The attenuation of adjacent harmonics is shown in figure 4(b) for a nominal 50Hz fundamental. New Zealand legislation requires that this attenuation be greater than 40dB [5]. It also states that harmonic voltage and current measurements shall be made when the system frequency is within 0.5 percent above or below the standard of 50Hz. Evaluating the attenuation for the two limits of 49.75Hz and 50.25Hz gives 46dB attenuation at each limit. Hence it is feasible to sample at a constant frequency for harmonic monitoring to comply with New Zealand legislation. However, the CHART harmonic monitor is equipped with a device [6] that produces a sampling signal of frequency f_s that is locked to the fundamental frequency f_0 such that $f_0 T_0$ is very close to unity, enabling CHART to monitor harmonics when the system frequency is well outside the limits set by New Zealand legislation. Because spectral leakage is reduced by sampling coherently with the fundamental, windowing of the time domain data prior to FFT computation is not necessary.

The FFT algorithm [4] is used to efficiently compute the DFT of voltage and current signals, and as discussed previously, the transform is computed over exactly one cycle of the fundamental. In this way, the system works on a cycle-by-cycle basis, treating each cycle separately, and producing harmonic results for each cycle. Harmonics up to the $50th$ are required, and in order to realise this, as well as satisfying the sampling theorem, the sampling frequency must satisfy the relation

$$f_s > 2 \times 50 f_0 \qquad (7)$$

where f_0 is the fundamental frequency. This corresponds to exactly 100 samples per cycle. The FFT algorithm requires a record length of $N = 2^\gamma$ samples, where γ is an integer [4]. The lowest value of N satisfying equation 7 is 128, meaning that 128 point FFTs are required to resolve up to the 50^{th} harmonic, giving a required sampling frequency of $128 f_0$ and 128 samples per cycle of the fundamental.

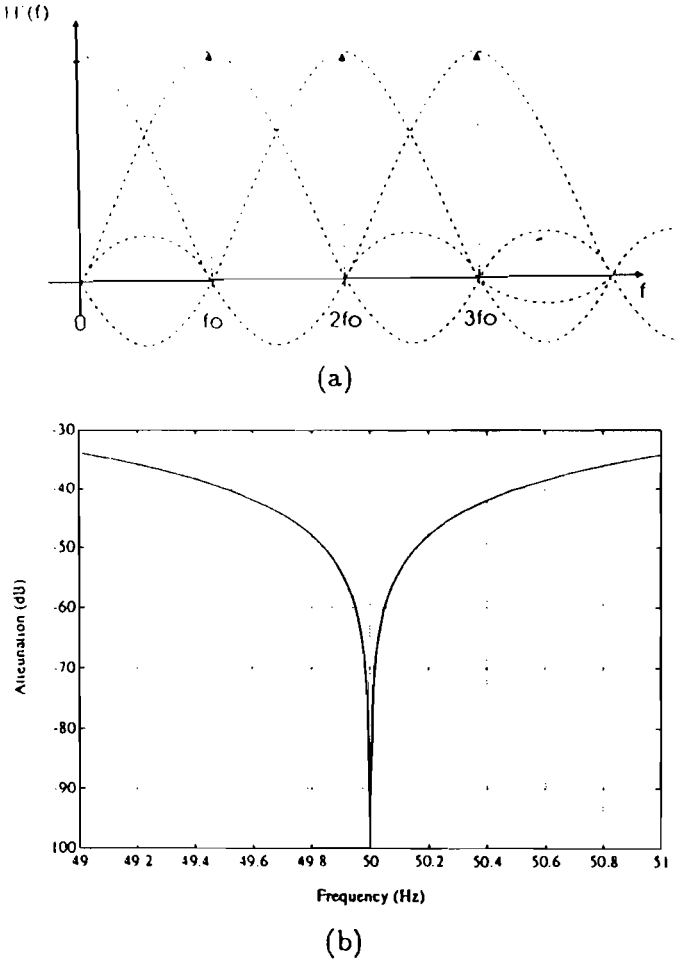

Figure 4: (a) The spectrum resulting from the rectangular windowing of a sampled signal. (b) The attenuation of an harmonic at an adjacent harmonic when the rectangular window is exactly equal to the period of the nominal 50Hz system frequency, but with the system frequency changing around the nominal 50Hz.

ANTI-ALIASING FILTERING

Sampling at a frequency of $128f_0$ - which is equivalent to $2.56f_{50}$, where f_{50} is the frequency of the 50^{th} harmonic - leaves a band between f_{50} and $f_s/2$ of unwanted harmonics in the FFT results, illustrated in figure 5(a). Because these results are not required, it does not matter if they are distorted by an anti-aliasing filter and by aliasing. Hence this band is used to implement an anti-aliasing filter with a roll-off from $f_c = f_{50}$ sufficiently steep to give 98dB attenuation at $f_s - f_c$, illustrated in figure 5(b). Aliasing will occur in this band, but because harmonic analysis is performed outside of it, it is of no consequence. The ADCs employed by CHART are 16 bit convertors, giving a theoretical RMS signal to quantization noise ratio of 98dB using equation 4.

The anti-aliasing filter required for the steep roll-off depicted in figure 5(b) can be realized by an analog filter, but is not practical in the CHART system which has physically small stand-alone low power data conversion modules [1]. The reasons for this are listed below:

- A passive analog filter requires much bulky circuitry and can be very sensitive to component variation.
- If built from active components its power consumption may be too high.
- Switched capacitor filters also consume too much power, and may cause significant harmonic distortion.
- Considerable phase and magnitude distortion will occur in the vicinity of the cut-off frequency, distorting important harmonic information.
- Ideally the group delay of the anti-aliasing filter should be constant, so that all harmonics are delayed by the same amount.

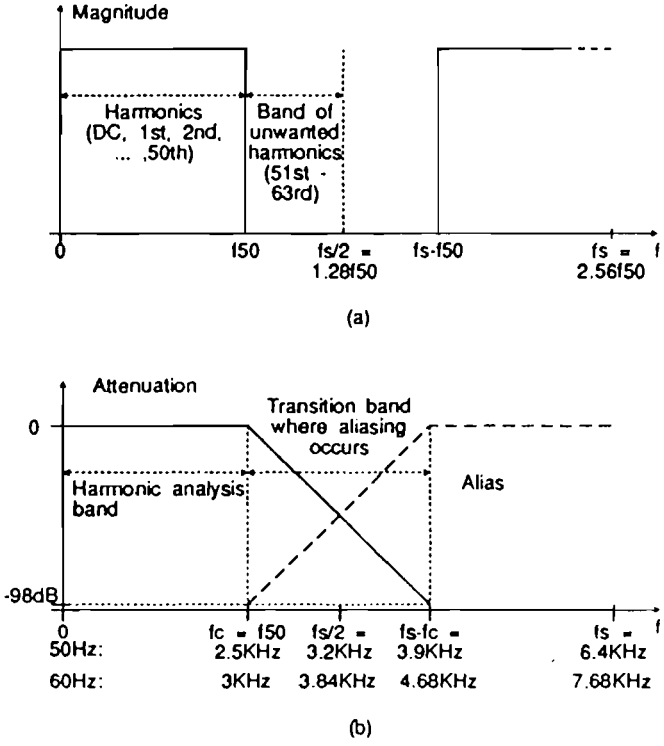

Figure 5: (a) Spectrum showing the band of unwanted harmonics resolved by the FFT. (b) The anti-aliasing filter response implemented inside this band.

The CHART instrument realizes this filter specification by using a digital FIR filter, implemented by each of its front-end DSPs, which are also used to find the FFT of each channel [1]. The analog voltage and current signals are sampled at a higher frequency than that required to give 128 samples per cycle. This reduces the required roll-off slope of the anti-aliasing filter preceding the ADC (illustrated in figure 6(b)), making its design much simpler. It can also improve the effective SNR of the sampled signal if the signal bandwidth is held constant [7]. This is known as *oversampling*, and is illustrated in figure 6(a), with the required anti-aliasing filter response preceding the convertor shown in figure 6(b).

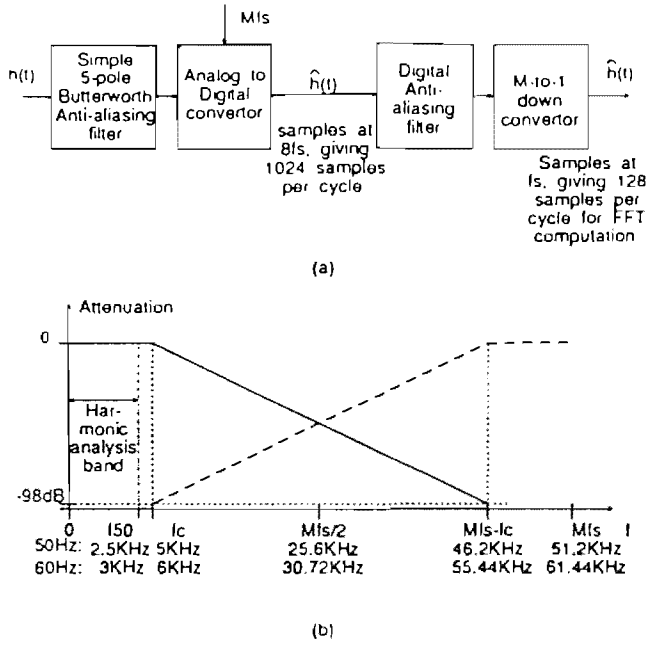

Figure 6: (a) Oversampling of a signal with anti-aliasing filtering performed by a digital filter. (b) The required filter response of an anti-aliasing filter preceding an oversampling ADC. Details for 50Hz and 60Hz power systems are shown below for an oversampling factor of $M = 8$.

The CHART instrument employs an oversampling rate of $M = 8$, resulting in a sampling frequency of $1024 f_0$. This enables a simple 5 pole Butterworth filter to be used as the front end anti-aliasing filter. A 5 pole Butterworth filter was used as it has a tolerably good amplitude response and a near constant group delay in the pass-band [8]. Due to its poor characteristics around the the cut-off frequency, it was designed to have a cut-off slightly above the $50th$ harmonic, minimising distortion to harmonics around the filter cut-off. An oversampling rate of 8 was settled on as a compromise between the analog filter being very simple (achieved with M large), and being able to perform a reasonable amount of computation by the DSPs (achieved with M small).
FIR filters have a number of features suited to this application. These are:

- Linear phase.
- Easy design and implementation.
- They are always stable.

Anti-aliasing FIR filter design

As discussed previously, the sampled signal $\hat{h}(t)$ must be re-sampled at a lower rate for FFT computation. Because it may contain frequency components beyond the now lower Nyquist limit when re-sampling (or down converting), it must be band-limited by an anti-aliasing filter. This is performed on the digital samples using a FIR filter. The implementation of FIR filters using DSPs is well documented [9], and the DSP used in the CHART project has an architecture and instruction set that can implement the convolution equation

$$y(n) = \sum_{k=0}^{N-1} h(k)x(n-k) \tag{8}$$

very efficiently [10]. This is the direct-form structure of the time-invariant FIR filter depicted in figure 7.

The frequency response of the filter required for anti-aliasing is depicted in figure 5(b). The filter coefficients, $h(k)$, were found from this response by essentially taking its inverse Fourier transform and modifying the resulting truncated impulse response by a Hamming window to reduce the Gibbs phenomenon [7]. The coefficients were then rounded for use in the 16 bit fixed point DSP [9]. The filter length was determined by two main factors, namely: the amount of processing time available on the DSP (the longer the filter the more processing is required), and how true the actual response is to be to the ideal response (the longer the filter, the better the response). The filter used in the CHART system has 128 taps, which is a good compromise between processing overhead and good response characteristics. Figure 8 shows the actual frequency magnitude response of the anti-aliasing FIR filter.

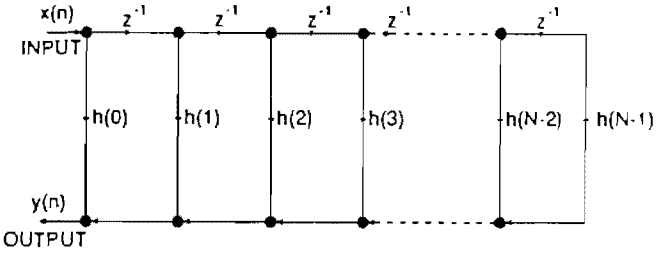

Figure 7: Direct form structure for a FIR digital filter.

For a 50Hz fundamental frequency, the sampling rate is $8 \times 6.4\text{KHz} = 51.2\text{KHz}$. To compute one output from the FIR filter of equation 8 requires N multiply and accumulate instructions, leading to $51.2 \times 128 = 6.5$ Million Instructions Per Second (MIPs) to implement the 128 tap filter. The DSPs used by CHART are capable of a maximum of 10 MIPs [10], and given that the 6.5 MIPs estimated to implement the 128 tap filter does not include any overhead, it is likely that the processor will not be able to complete an FFT in real-time after collecting 128 outputs from the filter. It must however be noted that the FIR filter is followed by an 8-to-1 decimator, meaning that the filter output need only be computed every 8th sample, theoretically reducing the MIPs required by the filter by a factor of 8 to less than 1 MIPs. Unfortunately this benefit is negated by the fact that the instruction set of the CHART DSP is arranged so that a multiply, accumulate, and shift is computed in one instruction, and although only every 8th sample requires a multiply and accumulate, all samples must be shifted in the filter shift register each time a new sample arrives - which happens at the higher sample rate.

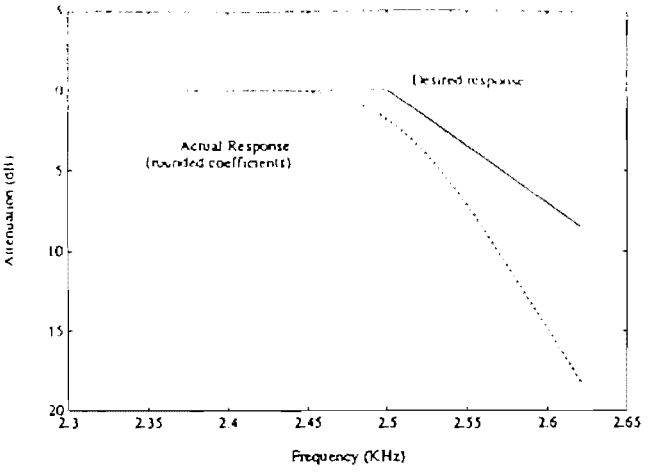

Figure 8: 128-tap Anti-aliasing FIR filter response for a 50Hz fundamental.

Clearly a more subtle approach is required to implement the filter efficiently. This approach involves breaking the filter up into a polyphase network, consisting of M smaller filters which contribute to the filter output for different time slots, and can be understood in terms of the *commutator model* , illustrated in figure 9 [7].

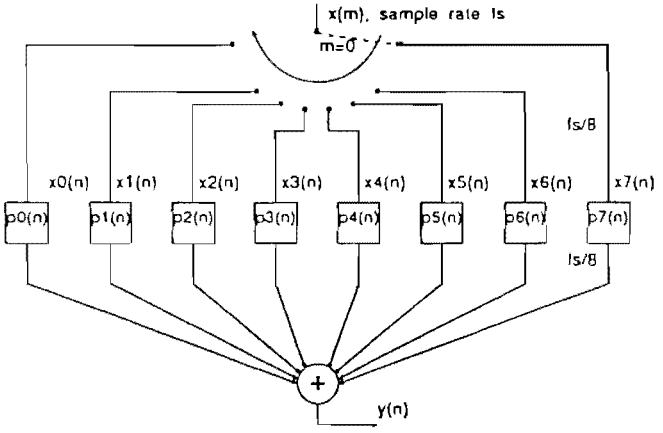

Figure 9: The commutator model for an 8-to-1 polyphase decimator. Each of the polyphase filters is a decimated version of the full filter impulse response $h(k)$.

The coefficients of the M-to-1 polyphase decimator are

$$P_\rho(n) = h(nM + \rho), \qquad (9)$$

for $\rho = 0, 1, 2, ..., M-1$, and all n, where ρ denotes the ρth polyphase filter. The commutator effectively takes M input samples of the signal $x(m)$ and distributes them to the polyphase branches in the reverse sequence $\rho = 7, 6, 5, ..., 0$. When each of the polyphase filters has received a new input, the polyphase filters are computed and their outputs summed to give a single output sample $y(n)$. This means that for each input sample (at a rate of f_s), only a $128/8 = 16$ tap filter needs to be computed, leading to $51.2 \times 16 = 0.8$ MIPs, which is significantly lower than the 6.5 MIPs required to implement the full filter. There is however a slight overhead in the implementation of the polyphase filter, although the DSP is quite capable of completing the FFT in the remaining time.

The FFT Implementation

As has already been discussed, the voltage and current signals are sampled coherently with the fundamental frequency, providing a finite set of samples in a form ready for analysis of spectral content by the DFT, using an FFT algorithm. They are also filtered sufficiently to ensure that aliasing will not distort spectral information, and decimated to a rate high enough to resolve up to the 50th harmonic, but not so high that unnecessary computation is performed in taking the FFT.

The task of finding voltage and current harmonic levels is consequently a straight forward implementation of the FFT on the DSPs. The most critical aspect is to ensure the integrity of the data as it flows through the system in real-time at multiple rates (illustrated in figure 10), and of the DSPs registers and accumulator as it switches between the filtering task and the FFT task.

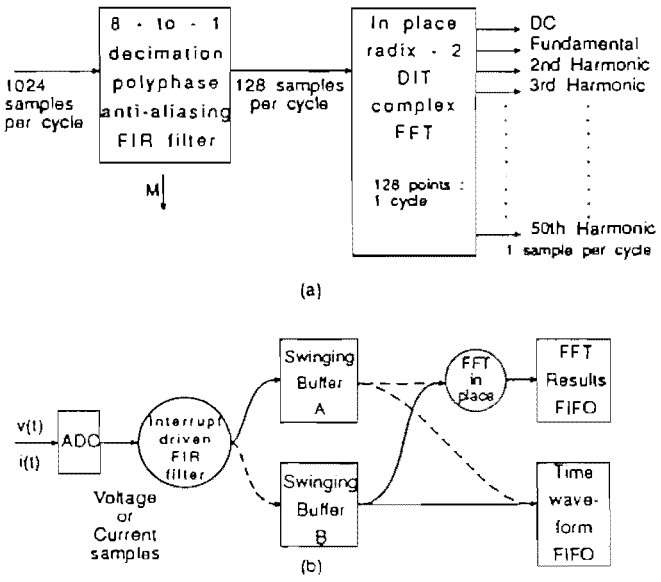

Figure 10: (a) Data flow in the DSP at various rates. (b) Data flow between tasks in the DSP.

Voltage and current signals acquired from transducers are real valued, which has two main implications. Firstly, the Fourier transform of the signals will have an even real part and an odd imaginary part, and secondly, it allows the butterfly operations in the first

two stages of the FFT to be stream-lined by using only real arithmetic [9]. Algorithms do exist that implement an N point real FFT by weaving the real input data into an $N/2$ complex input array [11]. The DFT is therefore computed with an $N/2$ point FFT, although the only advantage of this is a saving in memory space, as the butterflies at each stage must be general complex ones, and the output must be decoded, leading to approximately the same processing requirements.

The CHART project uses a full 128 point complex FFT to compute the DFT, setting the complex inputs to zero before the transformation is started. Computation is performed in place and in internal RAM to save memory and for extra speed [10]. Because the properties of the FFT output are known (due the input being real), only half the FFT output is required. A radix-2 algorithm [4] is used, as the bit reversing required by this can be performed automatically by the CHART DSPs [10], and a *decimation in time* algorithm is used so that the input to the algorithm may be bit reversed, rather than the output. The complex FFT output is converted to polar form, giving harmonic magnitude and phase. This required the implementation of a square root algorithm and ARCTAN algorithm on the DSP.

Figure 10(a) illustrates the FIR filter task and the FFT task performed by each of CHARTs DSPs, and the data flow between them at multiple rates. The FIR filter decimates the oversampled input from 1024 samples per 50/60Hz cycle to 128 samples per cycle. Subsequent FFT analysis on each set of 128 samples leads to a set of harmonics updated each cycle, giving one of each of the 50 harmonics (magnitude and phase) per cycle. The FIR filter is an interrupt driven task, with an operation by one of its polyphase filters performed each time a new sample arrives from the ADC (via the DSPs serial port [1]). The FIR filter output is stored in one of the swinging buffers depicted in figure 10(b), leaving a buffer free for FFT analysis, thereby ensuring no loss of data between tasks. The FFT is performed on the data from the free buffer when the DSP is not in the FIR filter interrupt service routine, and its results (harmonics) are placed in a hardware first-in-first-out (FIFO) buffer for use by CHARTs main processor [1]. The decimated time domain signal is also placed in a FIFO for use by CHARTs main processor. A "buffer swing" is performed once each cycle.

Each time an ADC sample arrives, the DSP must save its context from the FFT routine before servicing the sample and must restore the context before returning to the FFT. This adds a significant processing overhead to the DSP, as the ADC samples arrive at a high rate. Nevertheless, timing tests on the FIR filter and FFT operating independently and together indicate that the DSP is capable of implementing them in real-time. When performing a full context save and restore, the FIR filter takes 10mS to filter 1024 samples and produce 128 for the FFT. The FFT takes 2mS, including moving data from the swinging buffers into its in-place computation area (in the DSPs internal RAM), and moving the FFT results to the FIFO. The total time taken is therefore 12mS, corresponding to 72 percent of the available time for a 60Hz fundamental frequency, or 60 percent for a 50Hz fundamental.

CONCLUSION

The principles of filtering and sampling power system voltage and current signals for harmonic analysis using the FFT have been established, and their application in a practical instrument (CHART) has been described. The use of powerful digital signal processors in this instrument has enabled the implementation of multirate DSP techniques, leading to simplifications in data acquisition hardware, improved signal quality, and reduced computational requirements by the rest of the system. The multirate DSP techniques involved the innovative design of a polyphase decimation anti-aliasing FIR filter, and the implementation of an FFT algorithm.

The CHART instrument is a very flexible one, allowing DSP software developed on a PC to be downloaded to the CHART DSPs with minimal effort. This enables other harmonic analysis techniques to be tested easily making the instrument a powerful research tool. The technique described in this paper is only one of many that could be used for harmonic analysis, although it was found to be a very successful compromise between data acquisition hardware complexity and processing requirements.

Immediate plans for the development of harmonic analysis software using CHART are to increase the FFT record length beyond 1 cycle to 2, 4, 8, and 16 cycles, enabling the determination of inter-harmonic frequencies. The effect of averaging cycles will also be investigated. Other research activities with CHART involve its use in transient analysis, which requires sampling at even higher rates than those required for harmonic analysis, and using its DSPs to analyse transients on voltage and current waveforms.

ACKNOWLEDGEMENT

The authors acknowledge the financial support of TRANSPOWER N.Z. LTD., and A.J.V. Miller acknowledges the award of a 1989 UGC postgraduate scholarship. They also extend their appreciation to Malcom Barth and Dermot Sallis who assisted in the development of a working CHART prototype.

APPENDIX A

Consider

$$H'(f) = H(f) * \Delta_0(f) * T_0 \frac{sin(\pi T_0 f)}{\pi T_0 f} \quad (10)$$

which is the Fourier transform of the sampled and truncated signal $h(t)$ of figure 3(c).
Now if $h(t)$ is periodic it can be represented by a Fourier series expansion, with Fourier transform given by the equation

$$H(f) = \sum_{n=0}^{\infty} \alpha_n \delta(f - nf_0) \quad (11)$$

where α_n are the complex Fourier series coefficients [4].

If $h(t)$ is band-limited, this summation is over a finite number of harmonics from 0 to N (with the fundamental frequency equal to f_0). Substituting the Fourier transform of the bandlimited signal $H(f)$ into equation 10 yields

$$H'(f) = [\sum_{n=0}^{N} \alpha_n \delta(f - nf_0)] * \Delta_0(f) * \frac{T_0 sin(\pi T_0 f)}{\pi T_0 f} \quad (12)$$

Now since $h(t)$ is band-limited, if the Nyquist sampling criteria of equation 3 is met (that is, if aliasing does not occur), the base band signal alone can be considered (since this contains all the information necessary to reconstruct $h(t)$).

Expanding out the convolution with $\Delta_0(f)$ yields a base band term and spectra repeated at integer multiples of f_s. The base band term is

$$H'(f) = f_s[\sum_{n=0}^{N} \alpha_n \delta(f - nf_0)] * \frac{T_0 sin(\pi T_0 f)}{\pi T_0 f} \quad (13)$$

Convolving these two terms yields

$$\begin{aligned} H'(f) &= T_0 f_s \int_{-\infty}^{\infty} \sum_{n=0}^{N} \alpha_n \delta(\nu - nf_0) \frac{sin[\pi T_0 (f - \nu)]}{\pi T_0 (f - \nu)} d\nu \\ &= T_0 f_s \sum_{n=0}^{N} \alpha_n \frac{sin[\pi T_0 (f - nf_0)]}{\pi T_0 (f - nf_0)}. \end{aligned} \quad (14)$$

APPENDIX B

The contribution of harmonic n_1 at harmonic n_2 is given by the evaluation of $H'_{n1}(f)$ at $f = n_2 f_0$,

$$H'_{n1}(n_2 f_0) = \alpha_{n1} T_0 f_s \frac{sin(\pi T_0 f_0 [n_2 - n_1])}{\pi T_0 f_0 [n_2 - n_1]} \quad (15)$$

from equation 5 derived in appendix A. If $T_0 f_0 \neq n$, where n is an integer, $H'_{n1}(n_2 f_0)$ will be non zero at n_2, with an attenuation given by

$$A = \frac{H'_{n1}(n_2 f_0)}{H'_{n1}(n_1 f_0)}$$

$$= \frac{sin(\pi T_0 f_0 |n_2 - n_1|)}{\pi T_0 f_0 |n_2 - n_1|}. \quad (16)$$

That is, the interference of a signal at harmonic n_1 on harmonic n_2 will have an attenuation A, which is dependent on the separation of the two harmonics, but more importantly on how close $T_0 f_0$ is to unity, or how close the truncation interval is to an integer multiple of the fundamental frequency.

The attenuation for adjacent harmonics (where $n1 - n2 = 1$) in dB is given by

$$A = 20 log_{10} |\frac{sin(\pi T_0 f_0)}{\pi T_0 f_0}|. \quad (17)$$

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A.3 Satellite Time References Applied to HVdc Fault Location

92 SM 471-3 PWRD

THE APPLICATION OF SATELLITE TIME REFERENCES TO HVDC FAULT LOCATION

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Abstract - An HVdc fault location scheme is described which relies on very precise detection of the time of arrival of fault created surges at both ends of the line. Such detection is achieved by a very accurate data acquisition and processing system combined with the time reference signals provided by a global positioning system receiver. Extensive digital simulation is carried out to determine the voltage and current waveforms, to identify the main sources of error and suggest possible compensation techniques.

Keywords : HVdc, Fault Detection.

INTRODUCTION

HVdc transmission, like its ac counterpart, uses travelling-wave propagation times for the location of overhead line faults.

Two alternative implementations are in current use. One is the reflectometry technique [1][8][9][11], which measures the time difference between the arrival of the first surge and its subsequent reflections at one end of the line. It requires no information from the far end of the line and therefore needs no communication link between them.

This technique is attractive for its simplicity and low cost, but can not be relied upon for very accurate location under all possible fault conditions [9][11].

A more reliable technique is based on the time difference in the arrival of the fault-generated wave at each end of the line. Clearly the accuracy of this method depends on its ability to provide a common time reference at both ends of the line.

92 SM 471-3 PWRD A paper recommended and approved by the IEEE Transmission and Distribution Committee of the IEEE Power Engineering Society for presentation at the IEEE/PES 1992 Summer Meeting, Seattle, WA, July 12-16, 1992. Manuscript submitted August 26, 1991; made available for printing May 13, 1992.

In existing schemes, the problem is minimised by the provision of a dedicated microwave link to communicate the arrival of the surge at each end of the line [2]. This method provides immediate and accurate information, but it is expensive. Moreover, unlike fault detection which needs fast on-line action, fault location requires no immediate action and can be achieved off-line, provided a reliable absolute time reference is used at both ends. The general availability of the NAVSTAR GPS (Global-Positioning System) intersatellite receivers [3] provides a far more economical and accurate alternative to the microwave link and its application to off-line fault location is described in this paper. The NAVSTAR global-positioning system is a space based radio-navigation system developed by the U.S.Department of Defense, which also distributes precise time.

The objectives of this paper are fourfold. Firstly to propose the principles of the new method. Secondly to describe an instrumentation system that is capable of meeting the exact timing and data acquisition requirements of the method. Thirdly to identify the error sources and provide guidelines for establishing the limits of the key error contributions. Fourthly to describe the simulation studies used to investigate the error sources and the performance of the HVdc line and the instrumentation system under fault conditions.

FAULT LOCATION PRINCIPLE

The proposed fault locator is based on the detection of the arrival of the first wavefront surges (current and/or voltage) at both ends of the link. A first-order recursive digital filter and a threshold comparator are used for the detection, as shown below [1]:

$$e_i = Z_i - X_i \tag{1}$$

$$X_{i+1} = X_i + ke_i \tag{2}$$

where,

Z_i - measured quantity (current or voltage)
X_i - estimated value
k - a smoothing constant

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A line fault is indicated when the error e_i, which is equivalent to a differentiator-smoother output, exceeds the threshold value. A careful comparison of the dynamic response of the link to line and system faults is required in each scheme to decide the threshold levels to be used in such discrimination.

Accepting for the time being the existence of a perfect common time reference at both ends and the unambiguous detection of a line fault, both subjects to be discussed in the following sections, the fault distance of a perfectly homogeneous transmission line is given by the equation :

$$L_f = \frac{L}{2}(1 - \frac{(T_2 - T_1)}{\tau}) \qquad (3)$$

where,

T_1 - surge arrival time at the sending end
T_2 - surge arrival time at the receiving end
L - total length of the line
L_f - fault distance from the sending end
τ - travel time of the entire line

In practice, however, the geometrical and electrical parameters in a long distance transmission line will vary considerably along the line and a straight application of the equation (3) will result in considerable error as shown in the later sections.

INSTRUMENTATION SYSTEM

System Configuration and Operation

The instrumentation system to be used to perform the measurements for the proposed fault location technique is based on CHART (Continuous Harmonic Analysis in Real Time) [4][10]. As the name implies, this system is primarily aimed at harmonic measurements. However, by appropriate modifications to the data acquisition and processing software, the system is ideally suited to transient measurement. One of its main features is the inherent flexibility provided by system architecture which readily enables continuous on-line analysis of the captured waveform information on a number of channels.

Another key feature is the ability to accurately time stamp (to within a microsecond) the incoming data by means of a precision clock that is locked to the highly accurate GPS satellite timing signals. It is this time stamping accuracy that forms the basis of the fault location method.

A simplified block schematic of the instrumentation system as required at one end of a HVdc link is illustrated in Figure 1. The number of remote data conversion modules (RDCMs) can be chosen to suit the number of voltage and current transducers being maintained. Current and voltage signals from the current and voltage transducers are passed through signal conditioning circuits in the RDCMs of

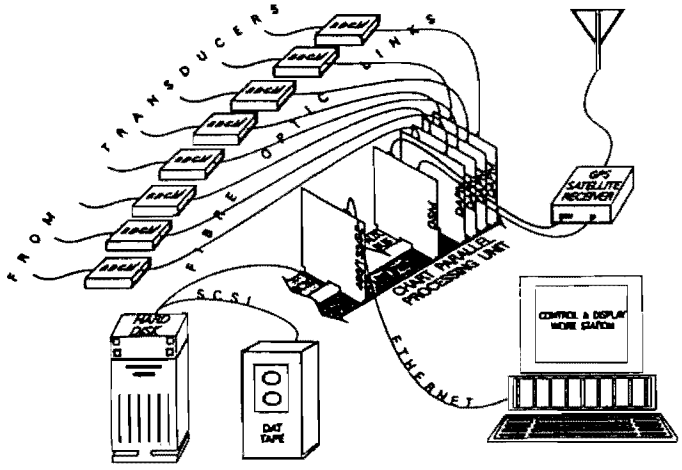

Fig.1: The CHART Data Acquisition and Processing System

the CHART system. These modules digitise the data under the direct control of the data acquisition and processing (DAPM) modules and the digital services module (DSM). The DSM provides the synchronised sampling signals and the precision system time clock signals to the DAPM units. The precision time clock signals are locked to the GPS satellite time reference as discussed later.

Communication between the RDCMs and their respective DAPMs is achieved by digital fibre optic links. The DAPMs relay the sampling signal to the RDCMs and control the serial data transfer from the RDCMs to their DAPMs. Time stamped packets of data are accumulated in rotating buffers within the DAPMs which also process the data to determine the arrival or otherwise of the fault wave front (the wave front detection algorithm). A positive fault arrival being detected will result in the transmission of the data packets containing this information to the central process control module.

The data packets then either await the arrival of corresponding data from the CHART unit located at the other end of the HVdc link, so that the fault position can be calculated or they can be themselves transmitted to the remote unit for similar processing. Alternatively data interchange can take place between both CHART systems enabling fault calculation at either end.

The CHART units provide storage facilities in the form of large disk drives and DAT tape units for storing all the acquired data - precisely what data is stored is directly controlled by the on-line storage analysis routines invoked by the user. For example a storage algorithm can be written which only stores data when a fault is detected, at which time it can store a predefined number of data packets containing information from both before and after fault occurrence.

The CHART system is provided with an ethernet bus interface. The prime purpose of this is to facilitate communication between the main CHART unit and its control and display workstation. It also enables communication with other CHART units and other display stations. If, as is now becoming prevalent, remote locations on a power system network are going to be provided with inter location ethernet wide area networks, then it will be possible to utilise these link for communicating fault wave front arrival information from one end of the HVdc link to the other. However the time taken to carry out this data transfer is not at all critical and can be done by any other data communication systems that exist including the public telephone or Integrated Services Digital Networks.

System Error Sources

There are several sources of errors that need consideration other than the precision system clock which is discussed in the next section. These include,

- transducer bandwidth limitations
- transducer signal conditioning circuitry bandwidth limitations
- A/D sample rate errors
- A/D conversion quantisation errors
- digital communication (fibre-optic) propagation delay errors
- wavefront detection algorithm errors

Propagation delays both through the analog and digital circuitry can in general either be compensated for or eliminated by subtraction. If identical sets of transducers and interface circuitry are used at either end then to some extent timing errors from this source are self cancelling. Limited bandwidth on all or some of these components will basically result in corresponding transient rise time delays. The effect of these delays on timing error will be most evident for faults occurring close to either end of the HVdc link. Clearly the limited bandwidth of the transducers and the associated circuitry will have a more significant effect on the very fast rising wave front than it will have on the much slower one. For conditions where the fault occurs nearer the middle of the HVdc link the fault waveforms arriving at either end will have similar rise times and the limited bandwidth of the receiving transducers and circuitry will again be self cancelling.

The sample rate and quantisation errors result from the analog to digital conversion process. In general the higher the sample rate and the smaller the quantisation level the more accurate is the determination of the wave front arrival time. There are practical limits to these parameters both in terms of what can be physically realised and the cost of implementing the circuitry.

The HVdc fault location simulation studies reported later in this paper are able to assess the effect of both sample rates and quantisation levels on wave front arrival timing accuracies. As a result of these tests, guidelines can be provided for the optimum choice of these parameters.

The system schematic in Figure 1 shows that there is a fibre optic link between the RDCM and its DAPM. This link in itself can introduce significant propagation delays (approximately 3 nanoseconds per metre or a microsecond for 300 metres). Furthermore the associated logic circuitry can also add its propagation delays. The time stamping function carried out in the CHART system is directly linked to the digital conversion sampling signals. Consequently the main timing error from this source will be the time taken to propagate the sampling signal through the fibre optic link to the RDCM. This error can be accurately estimated and compensated for or alternatively, providing the system configurations at either end of the HVdc link are identical (including fibre optic line lengths), they will also be self cancelling.

The wave front detection algorithm must be able to detect the wave front arrival, establish its arrival time and, ideally, provide some level of discrimination against false signals. The main difficulty here is the wide dynamic range of fault signals that have to be catered for. This in turn is a direct function of whether the transducers directly provide either the voltage/current signals or the rate of change of these signals.

Precision Time Source Errors

The GPS satellite system consists of a network of 18 to 24 low orbiting satellites which, for a final operating constellation of 21 satellites, will be able to guarantee to provide positional and timing information from more than one satellite to any point on the globe, 24 hours of the day. The GPS satellite receiver acquires timing and positional information from typically three to six satellites of the GPS system which are visible at any one time. By appropriate computation on all the incoming signals from the satellites it is able to very accurately compute its position and provide the highly accurate 1 pulse/second timing pulses. The "absolute" time (from year down to nanoseconds) of these pulses is provided via a separate serial communication output from the receiver. Depending on the design of the receiver it is possible to have accuracies of ± 50 nanoseconds [5].

Even if the accuracy of positional information available to standard users is reduced by a factor of 3 or 4, the timing accuracies available will still be ± 175 nanoseconds. The CHART system itself has a temperature stabilised precision clock which locks on to the satellite receiver pulses to provide a system clock which is within ± 100 nanoseconds of the satellite receiver time. Thus assuming a normal distribution for these two timing error sources it is estimated that

nominal time stamping error will be typically ±200 nanoseconds. Consequently, even with this degradation and taking into account that there are two wave front arrival times being determined, errors in estimating fault location resulting from timing errors should not typically exceed 85 metres or 170 metres to a 95% confidence level.

SIMULATION PERFORMANCE

Simulation Tools

The steepness of the wavefronts expected at the line terminations requires accurate modelling of the frequency dependence in the components involved. Also, the line resistance is high due to skin effect in the conductors and should be accurately represented.

The ATP version of the EMTP program is selected for the studies which includes JMARTI line model [6]. This model can handle resistances as truly distributed and can take the frequency dependence of resistances and inductances also into account.

Test System

The New Zealand bipolar HVdc link is used as a test system in the digital simulation [7].

The dc link shown in Figure 2 consists of 535 km of overhead line followed by 40 km of submarine cables. Since the object is to provide a fault locator for the overhead line, the line can be considered to be terminated by the cable at one end and by the convertor terminal at the other end.

However, as the primary interest of the proposed fault location is to detect the surge wave-fronts arriving at the line side of the smoothing reactor, it is not necessary to model the ac system and the convertors in detail and the effect of convertor control is ignored. A series of sensitivity studies were carried out to decide on convertor model complexity. Figure 3 shows the components considered at the convertor terminals, i.e. smoothing reactor, dc filters, surge capacitors and power line carrier communication capacitors.

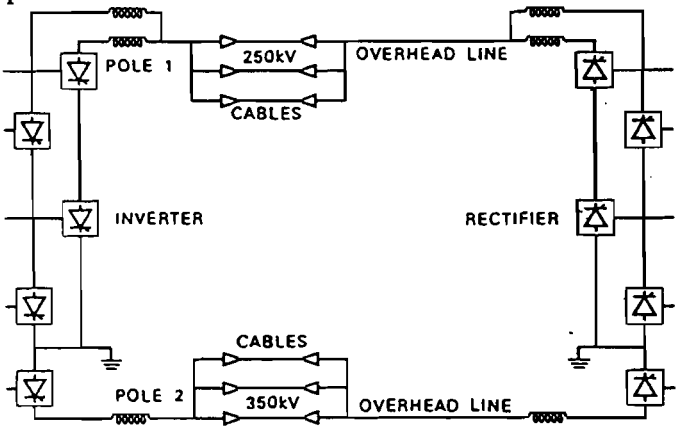

Fig.2: Test system

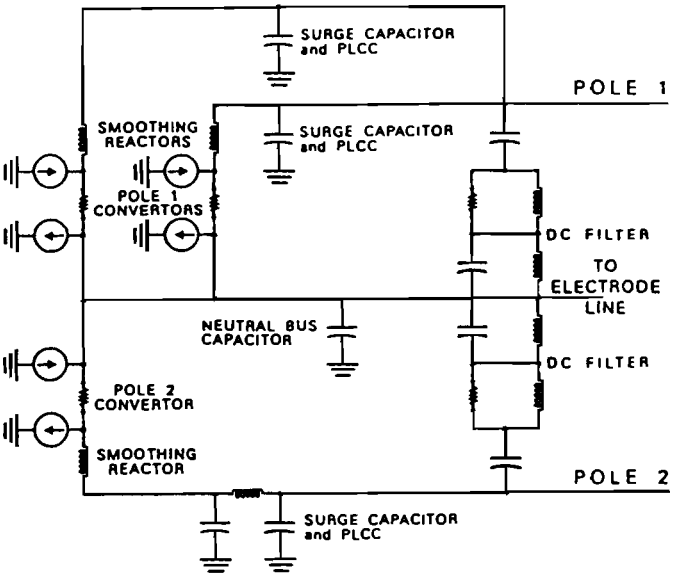

Fig.3: Convertor terminal components modelled

The overhead line is of non-homogeneous nature due to the use of two different types of towers and the considerable differences in earth resistivities along the line.

The submarine cables are separate from each other and hence they have been represented as single phase distributed transmission lines with and without frequency dependence for comparison. The first surge results of the two alternative models were indistinguishable.

Effect of Earth Resistivities

Usually the earth resistivities are not uniform over the entire length of the line and often such data is not available. In order to find the effect of this factor on first surge, a sensitivity study has been carried out for the test system.

The test system overhead line is a bi-polar line and hence has two different modes of propagation, i.e metallic and ground modes.

The propagation velocities of metallic and ground modes with respect to speed of light for the overhead line were calculated at various frequencies and earth resistivities and the results are shown in Tables 1 and 2. It can be seen from the tables that the ground mode travels much slower than the metallic mode and hence the propagation velocity of surge wavefronts is basically governed by metallic mode.

Table 1: Metallic mode velocities for different earth resistivities

f (Hz)	$\rho = 300\Omega m$	$\rho = 1650\Omega m$	$\rho = 3000\Omega m$
5	0.94450	0.94450	0.94450
50	0.98525	0.98525	0.98525
500	0.99175	0.99175	0.99175
5,000	0.99617	0.99614	0.99613
50,000	0.99779	0.99762	0.99759
500,000	0.99863	0.99833	0.99823

Table 2: Ground mode velocities for different earth resistivities

f (Hz)	$\rho = 300\Omega m$	$\rho = 1650\Omega m$	$\rho = 3000\Omega m$
5	0.64277	0.61476	0.60574
50	0.72895	0.69897	0.68953
500	0.86164	0.83619	0.82829
5,000	0.90557	0.87483	0.86499
50,000	0.9497	0.91861	0.90728
500,000	0.97992	0.95976	0.95028

It can also be seen from the tables that the metallic mode velocities are practically the same, irrespective of earth resistivity values.

Effect of conductor Height

The calculation of line parameters for the digital simulation requires the average conductor height between two towers. However, the average conductor heights are not uniform due to variations in tower distances and conductor sag.

A sensitivity study was carried out to find the effect of average conductor height on the simulation results. Metallic mode velocities were calculated for the test system overhead line by considering no sag and a sag of 10 metre and the results are shown in Table 3. The velocities are again practically the same in both cases.

The above results indicate that the effects of earth resistivities and conductor heights are not very significant as far as the calculation of the arrival of the surge wavefronts is concerned.

Table 3: Metallic mode velocities with and without sag

f	metallic mode	
Hz	no sag	sag = 10m
5	0.94450	0.94366
50	0.98525	0.98438
500	0.99175	0.99087
5,000	0.99614	0.99525
50,000	0.99762	0.99674
500,000	0.99833	0.99755

Effect of Sampling Frequency

The calculation of fault distance using equation (3) does not take the digitisation of electrical quantities by A/D convertors into account. The error introduced by the finite sampling rate is assessed with reference to a fault placed 23.9 km from the line terminal.

Assuming that the fault locator's digital sampler is limited to 50 kHz, the use of the same sampling rate in the simulation (i.e an integration time step of $20\mu s$) produces the results plotted in dotted line in Figure 4.

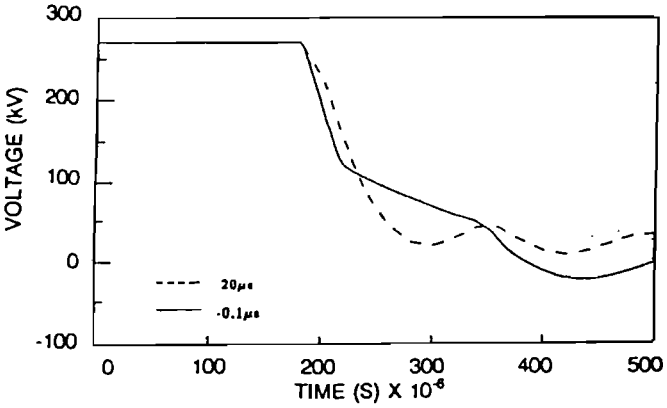

Fig.4: Convertor terminal voltage for $20\mu s$ and $0.1\mu s$ time step

If instead the sampling frequency of the simulation is increased to 10 MHz (i.e an integration time step of 0.1μ), the results are substantially different, as shown in Figure 4 in continuous line. Hence, irrespective of the sampling frequency of the data acquisition system, a very small time-step (in the order of $0.1\mu s$) should be used for the simulations.

The effect of differentiator-smoother circuits are also represented in the simulation. The voltage and current waveforms derived at the terminals are passed through these circuits whose output are compared with corresponding threshold values to detect a surge arrival.

Figure 5 shows the differentiator-smoother output for different sampling frequencies at the sending end for the same fault location. It can be seen from the figure that the differentiator-smoother output also depends on the sampling frequency and so the threshold value for discrimination should be chosen for a particular sampling frequency.

The calculated fault distance using the travel time based on the speed of light and with a sampling frequency of 10 MHz was 23.4 km, which is in error by 500 m. Assuming that the calculated fault distance should be accurate for this high sampling rate, then the per-unit propagation velocity is calculated to be 0.99797. According to Table 1, this velocity would correspond to a frequency of a few hundred kHz. Therefore, this velocity has been used for the calculation of fault distances for the remaining cases.

Table 4 shows the error in calculated fault distance for two extreme cases of fault location. The

Table 4: Error in located fault distances for various sampling frequencies

Sampling	Error in located distance in km	
Frequency	Fault at 23.9 km	Fault at 513.8 km
10 MHz	0.0	0.005
1 MHz	0.404	0.249
100 kHz	1.093	0.698
50 kHz	1.901	2.195

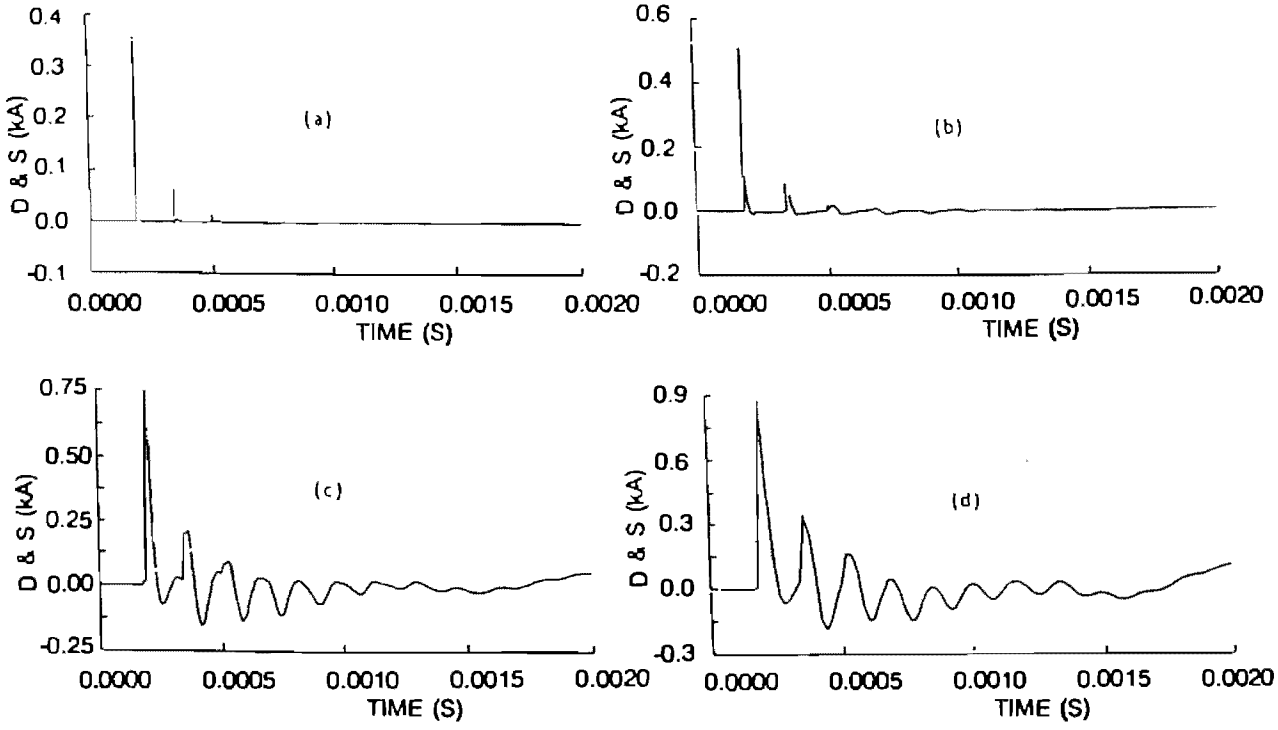

Fig.5: Differentiator-Smoother output with sampling frequencies of (a) 10 MHz (b) 1 MHz (c) 100 kHz (d) 50 kHz

close fault (23.9 km from the convertor plant) is assummed to have a 1 ohm fault resistance. The distant fault (513.8 km from the convertor) is specified with 20 ohm fault resistance.

The table shows a maximum error of 2.195 km (or 0.41% of line length) for the distant fault calculated with the lowest sampling frequency (50 kHz). Figure 6 shows the the errors in located fault distance with respect to sampling frequencies, from which it can be seen that a sampling freqency of at least 500 kHz should be chosen to keep the error within 500 metres.

Effect of Temperature Variation

The fault distances calculated according to equation (3) are based on the assumption that the conductor sags are uniform. On the other hand, the conductor sags are temperature dependent. If the temperatures along the line are known, then it is possible to compensate for them during the calculation of the fault distance.

In order to calculate the actual local lengths, the entire line is divided into various zones which can be considered to have specific average temperatures at the time of fault. If the line is divided into 'm' zones according to the temperature, then the actual fault location L'_f is given by,

$$L'_f = L_f - \frac{L_f}{L}\sum_{i=1}^{m}(l_{si} - l)n_i \qquad (4)$$

where,

l_{si} - conductor length per span in i^{th} zone
l length of the span
n_i - number of spans in i^{th} zone
L_f - fault distance calculated from equation (3)

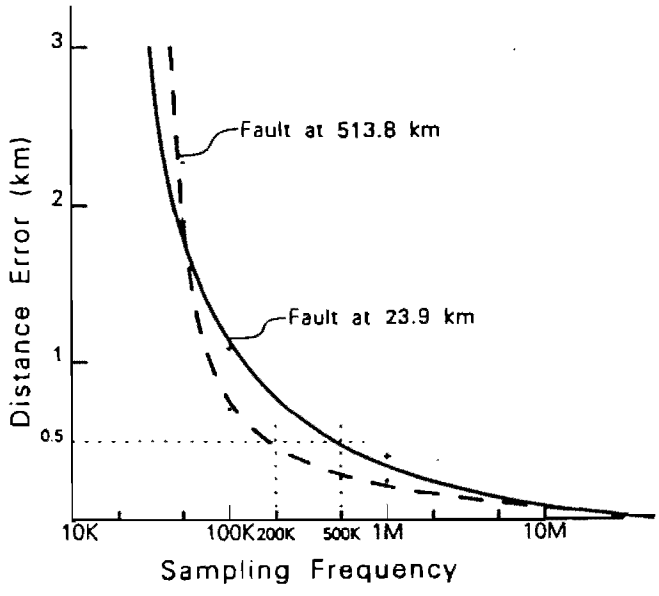

Fig.6: Error in located fault distance with respect to sampling frequency

To illustrate the effect of temperature variations, the test system line is divided into two nominally equal zones on either side of the fault. It is assumed that there is a mean temperature differences between the two zones of 20 degrees. The difference in calculated distance with equations (3) and (4) is found to be 2.1 km (0.39% of the line length). Consequently, providing suitable temperature information can be obtained, errors from this source can be calculated as per equation (4).

CONCLUSION

The principles of estimating the fault location by measuring the relative times of the fault wavefronts' arrival at either end of a transmission line is simple in concept but demanding in its implementation. The method relies on having, at both ends, highly precise synchronised time clocks, a requirement made possible by the use of time reference signals from the GPS satellite system. The voltage and current wavefronts are processed by CHART, a very accurate data acquisition and processing system. Error sources have been identified and can be divided into two main groups.

Those that are a function of the fault wavefront propagation speeds along the transmission line and result from the variations in the physics of the transmission line, its terminations and the environmental factors - these errors are present irrespective of the method used to locate the fault. The usefulness of digital simulation to investigate these effects has been demonstrated and it has been shown that the major contribution to these errors comes from temperature variations along the line. While these can in theory be compensated for, in practice the realities of establishing exact temperature profiles make such compensation difficult.

The other main group of errors is that resulting from the elements of the instrumentation system. The scope of these errors has been identified for the proposed instrument system configuration. It has been shown that some errors can be compensated for or can be self cancelling. The contribution of timing errors from the precision clocks has been established and shown to be relatively low and acceptable. The importance of the sampling rate and, to a lesser extent, quantisation levels of the analog to digital conversion circuitry has also been demonstrated. Preliminary indications are that sample rates of 500kHz with quantisation levels equivalent to 8 bits provide adequate performance. The value of the simulation studies in establishing these guidelines is very evident and further extensions to these studies are planned.

Another major error source is the noisy environment of the instrumentation system. Due to this noisy convertor environment, further work is being carried out on the design and location of the transducers; the intention is to place them sufficiently apart from the convertor terminal to provide better discrimination. Furthermore, the fact that the system is only concerned with the dominant initial fault wavefront means that higher thresholds of detection can be set, thus providing better noise immunity.

The implementation of this system on the new HVdc link in New Zealand is now being planned for early 1992 and will be appropriately reported on. The studies reported on here indicate that this technique has the potential for having a better performance than existing methods and is significantly less expensive.

ACKNOWLEDGEMENTS

The authors wish to thank TRANSPOWER NZ LTD. for the financial support provided to carry out this project. They also wish to thank their colleagues A.Miller, M.Livingston, S.Chen and C.Meyer.

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A.4 Harmonic Measurements on the NZ Power System with CHART

HARMONIC MEASUREMENTS ON THE NEW ZEALAND POWER SYSTEM USING CHART - A CONTINUOUS HARMONIC ANALYZER IN REAL TIME

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Abstract - This paper initially provides a brief overview of the design and development of the CHART (Continuous Harmonic Analysis in Real Time) system which has been developed by the authors in the EEE Department of the University of Canterbury for the purpose of carrying out continuous harmonic measurements in real-time on power systems. The paper then goes on to report on the actual field tests using this equipment on the New Zealand Power System. The report verifies that the laboratory prototype of CHART could be successfully used for field tests and identifies all the practical problems associated with such an exercise. In particular the practical issues associated with interfacing such equipment to the power system Voltage and current transducers via fibre-optic links are described together with details of the necessary on-line compensation for the characteristics of the transducers, fibre-optic links and associated signal conditioning circuitry. The ability of the CHART system to continuously monitor and analyze harmonic information in real-time (a feature not present in any other known equipment worldwide) is demonstrated. The limitations of the monitoring system are identified and proposed improvements to the system are discussed. The paper concludes with a brief description of the new CHART II system which is currently under development.

1 INTRODUCTION

Non linear loads in a power system such as large static AC/DC power convertors result in distortion of Voltage and current waveforms from their ideal sinusoidal shapes. This distortion is analyzed in terms of harmonic levels, where an harmonic frequency is an integer multiple of the power system fundamental frequency (nominally 50 or 60Hz). Harmonic Voltages and currents present on a network can have a profound affect on its operation and management by stressing equipment, leading to its de-rating or possibly even its destruction, and can interfere with telecommunication circuits by electromagnetic induction of audible tones.

Many countries including New Zealand that have experienced harmonic related problems, have introduced legislation to limit harmonic levels. However, the

legislation can only be policed if harmonic monitoring instrumentation complying with the legislation exists. Specifically, New Zealand legislation requires that Voltage and current levels as high as the 50th harmonic be resolved. It also requires the computation of total harmonic Voltage distortion, equivalent disturbing Voltage, and equivalent disturbing current [1]. Additionally, present experience with harmonic measurements indicates that the levels found in the three phases of a power system are always different, and therefore the simultaneous detection of multiphase information is essential for thorough investigation. The speed of monitoring is not critical in detecting what is generally steady state waveform distortion. However, gathering information in real-time could be used to take instant action upon the detection of unusual levels of non characteristic harmonics. It is also important to be able to measure harmonic levels continuously on a cycle by cycle basis to examine short term variations in harmonic levels caused by transient events such as starting a motor with a power electronic motor speed controller.

The CHART harmonic monitor has been designed to meet all of these requirements, and is therefore a very general instrument with a tremendous number of potential applications in harmonic measurement. In this respect it is also superior to other harmonic monitors which are generally only capable of snap shot measurements on up to two channels. After a brief overview of its structure and salient features, this paper documents the harmonic measurement field trials of a preliminary version of the CHART harmonic monitor (CHART I) at the Islington substation 220KV bus. It then concludes this discussion by summarizing changes to the harmonic monitoring instrumentation design leading to a much improved monitor (CHART II). The improved design was conceived by the authors over several months as a result of the preliminary field trials and visits to Intel in the USA and to the 1990 4th International Conference on Harmonics In Power Systems in Hungary. It has been developed since then to the stage where a workable prototype is now being produced. Finally it discusses future applications of CHART II.

2 AN OVERVIEW OF THE CHART I INSTRUMENT

The CHART I system used to make harmonic measurements is based on the Intel Multibus II bus architecture [2], is reported in [3], and is outlined in figure 1.

Briefly, the data acquisition system acquires six analog Voltages simultaneously from external power system transducers and converts them to digital samples. The digital samples are acquired by a Multibus II 186 computer, which also averages the samples over 5 cycles of the fundamental. The averaged cycles are transformed to harmonic data by the Multibus II 386 computer using an FFT, and the resulting data is compacted and archived to disk by a 286 Multibus II computer and transmitted to a PC-AT for display. Data transfer between

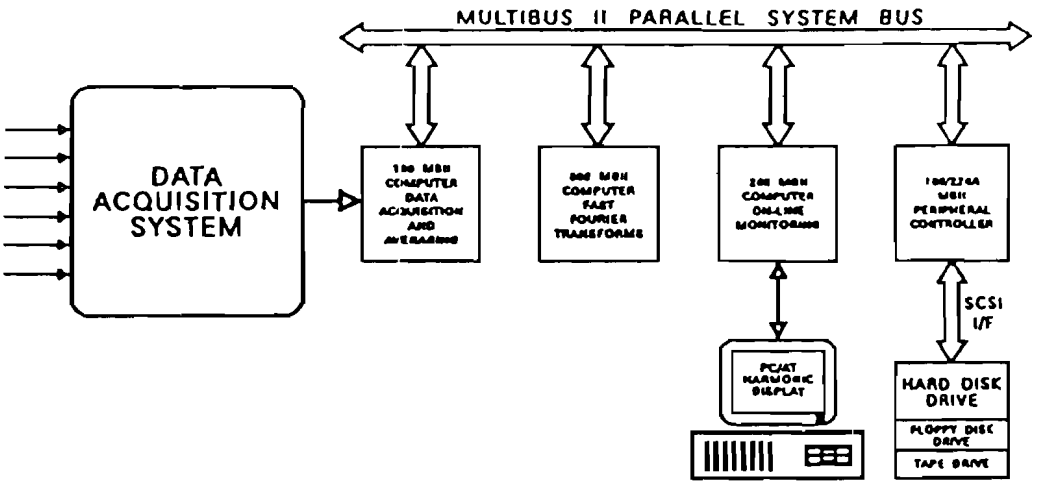

Figure 1: The CHART I harmonic monitoring system.

Multibus II computers is over the Multibus II parallel system bus.

The data acquisition system samples all channels simultaneously, with the sampling rate synchronized to the fundamental frequency - a technique often referred to as *quasi synchronous sampling*, and adopted by almost all AC power system harmonic analyzers [4], [5], [6]. This significantly reduces *spectral leakage* from the FFT [7], thereby avoiding the need to window the time domain data. Synchronous sampling also enables *coherent averaging* [8] of multiple cycles, which is similar to taking the FFT over multiple cycles, although it only resolves harmonic frequencies, leading to a significant reduction in the computation required to transform the data.

For the 1990 field trials, the system was configured to continuously compute the harmonic levels of six channels over five averaged cycles to comply with New Zealand legislation [1]. This allowed simultaneous measurement of Voltage and current harmonic levels on all three phases of the transmission line. The resulting harmonic data was then monitored to give peak harmonic levels for one second intervals, 10 second intervals, 1 minute intervals, 10 minute intervals, and 1 hour intervals. This data was then stored on a hard disk along with the time that the data was measured, and the power system fundamental frequency at the time of measurement. Harmonic level results were also sent to the PC-AT display system for immediate inspection, along with time data, and the fundamental frequency.

3 HARMONIC MEASUREMENTS USING CHART I

With the cooperation of the Electricity Corporation of New Zealand, the prototype CHART I system was used to monitor harmonic levels at the Islington end of the Islington - Twizel 220KV transmission line. Design Power New Zealand's fibre optic harmonic monitoring system was used to isolate the instrumentation from Voltage and current transformer connections in the Islington switchyard, as illustrated in figure 2 [9]. Figure 3 shows the location of the current transformers (CTs) and the Voltage transformers (VTs) used for the tests on the transmission line. Conventional protection CTs and CVTs were used to provide replicas of the line current and Voltage waveforms. These have unknown low pass frequency responses which will have affected the results obtained - especially the Voltage harmonics [10], [11]. However there was no alternative, and as the purpose of the exercise was to evaluate the system rather than the end results, these were considered adequate. Due to data storage limitations of the system as it was configured then, harmonic levels were only monitored and stored for up to one hour. This was performed several times throughout the tests, storing the results on DAT tapes at the end of each session.

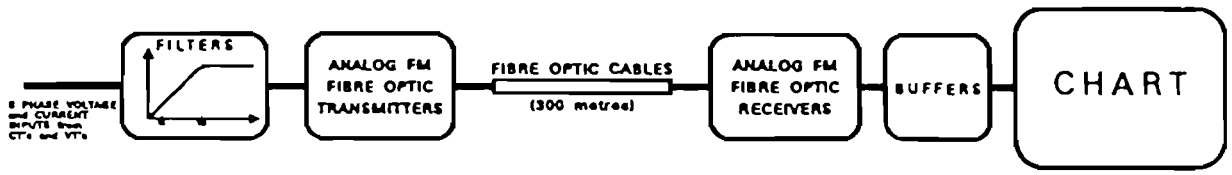

Figure 2: CHART I harmonic monitoring instrumentation setup.

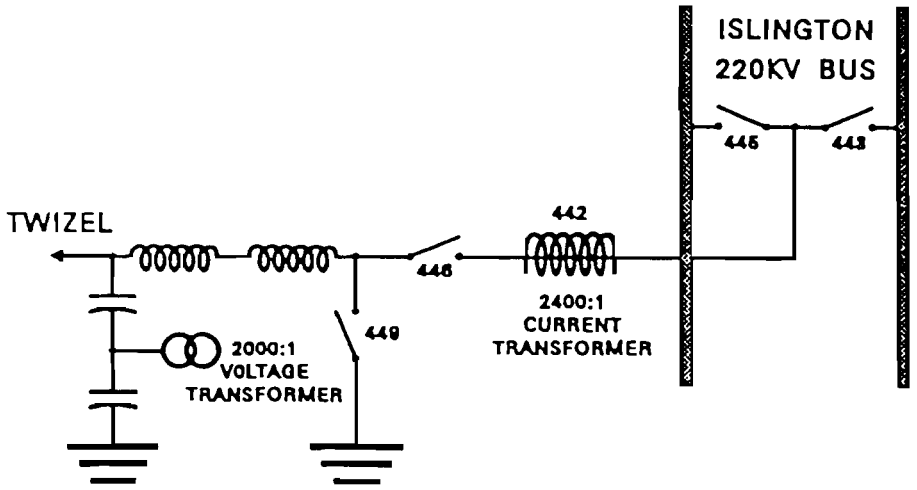

Figure 3: Current and Voltage transformer locations used for testing.

3.1 The limitations of present measurement techniques

The Design Power harmonic measuring fibre optic system is an analog FM system specifically intended for analysis of signals on in-service high Voltage equipment. This transmission system has a signal to noise ratio which is too low for the reliable determination of Voltage and current harmonic levels when transmitting the fundamental. This problem is circumvented by preceding the transmission system with high pass filters designed to attenuate the fundamental frequency, thereby raising the measured signals harmonic levels above the noise floor of the available transmission channel [12]. High pass filtering is a recognized technique for use in systems with a limited signal to noise ratio [13], although it requires compensation for the filter responses - another computational burden and source of error. Compensation for the filters was achieved by multiplying harmonic magnitudes by lookup tables, determined from the filters in the laboratory. The phase response of the filters was compensated for by adding the inverse filter phase responses to the harmonic phase results - also determined in the laboratory [9]. Unfortunately these high pass filters attenuate the fundamental component so severely that it is extremely difficult to reliably amplify it back to its original level given that the fundamental frequency of a power system varies continuously [9]. Nevertheless, it must be stressed that this system is adequate for assessment of compliance with present New Zealand legislation which does not require the fundamental component [1]. However, for more thorough research the fundamental component is important [14].

3.2 Harmonic current and Voltage results

A major difficulty with harmonic monitoring is the huge amount of data it produces. For instance, to store the results of monitoring up to the 50th harmonic of six channels over 5 cycles for one hour would require 44 Mega bytes of storage. Considering that some investigations require monitoring for many weeks, to store all of the results is not practicable. It is also questionable why the data should be stored - obviously it would take a long time to examine it. It is therefore necessary to present the data in some easily comprehended form that requires minimal storage. The approach adopted in the use of CHART was to record the maximum level that occurred over a pre-defined time span (say one minute). From this data, trends in harmonic levels over time can be easily graphed by displaying harmonic Voltage or current versus time, as illustrated in the results of figure 4. These figures show the maximum harmonic Voltage and current levels for the RED phase over 10 second intervals. Shown beside each "scratch" graph is a histogram, giving the occurrence of a particular harmonic Voltage or current. Histograms are an efficient way of storing harmonic levels

measured over a large time span. However, they give no indication of the time of occurrence of the harmonic levels, and of the power system state when the various harmonic levels occurred. Ideas for improvements on this are discussed in section 4.

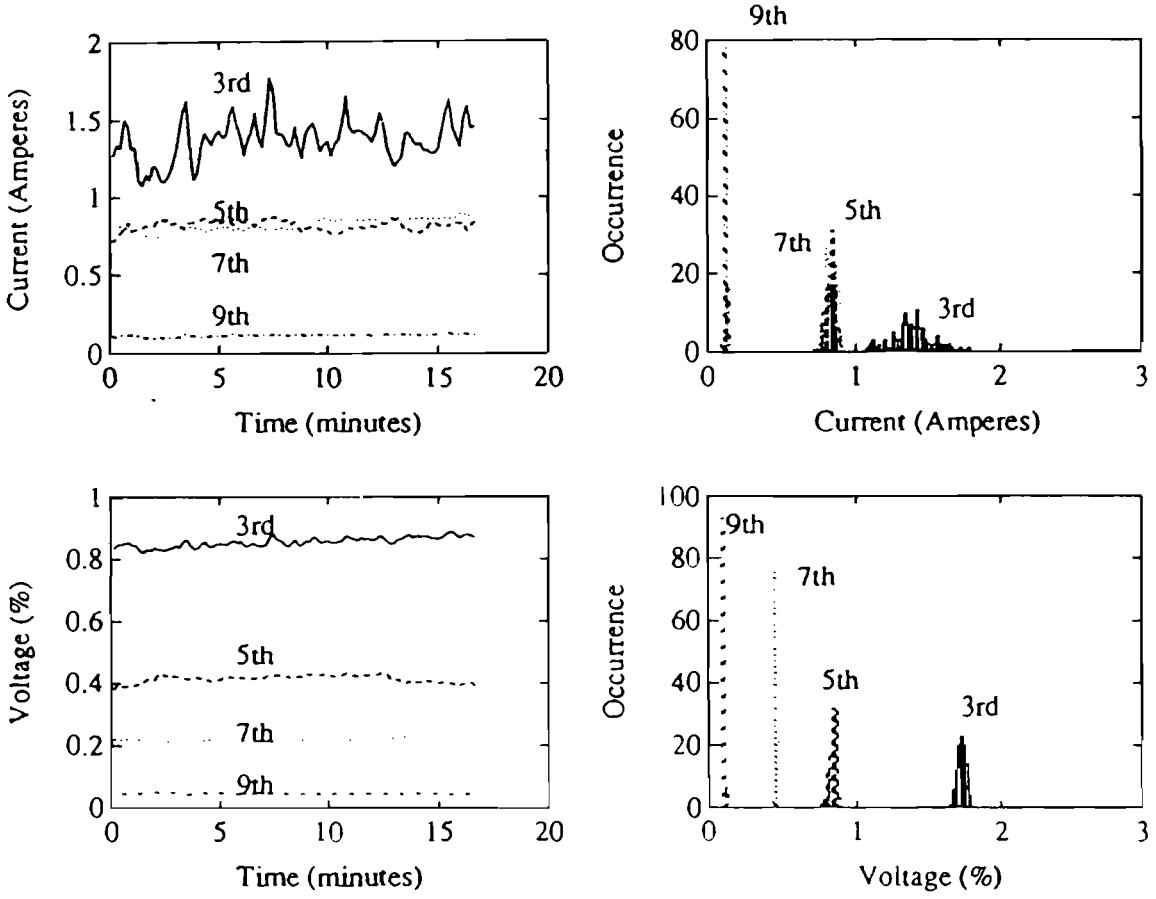

Figure 4: Selected red phase Voltage and current harmonics measured at the Islington substation on the Islington-Twizel 220KV transmission line, beginning at 2pm, Thursday July 26, 1990. Current is shown in Amperes and Voltage is shown as a percentage of the nominal system phase to Earth Voltage.

During monitoring, instantaneous harmonic magnitudes for all three phases up to the 50th harmonic can be displayed on a single chart, as illustrated in figures 5 and 6. Readily apparent from the charts is that the blue phase 3rd harmonic Voltage is significantly lower than that of the red and yellow phases - illustrating the importance of three phase harmonic measurement and display.

3.3 Harmonic impedance and power

Harmonic impedance data of a supply system is of importance to supply authorities and consumers, as high harmonic impedance can indicate a possible

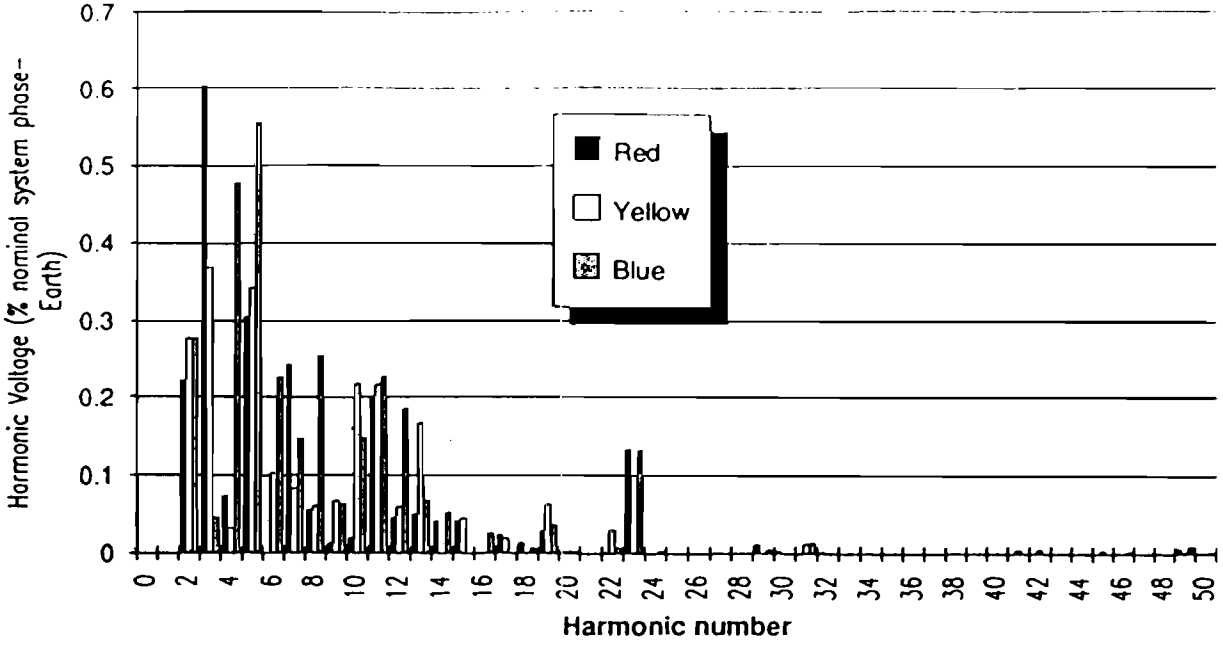

Figure 5: Harmonic Voltages measured at the Islington substation on the Islington-Twizel 220KV transmission line, 1:30pm, Wednesday July 25, 1990.

resonant condition which could lead to the amplification of harmonic Voltages. Given that the CHART harmonic monitor can compute harmonic Voltage and current at a busbar (both magnitude and phase), it is possible for it to compute harmonic impedance at a busbar [14], given by

$$\tilde{Z}_n = \frac{\tilde{V}_n}{\tilde{I}_n} \tag{1}$$

or

$$\tilde{Z}_n = \frac{V_n}{I_n} \angle \phi_{vn} - \angle \phi_{in}, \tag{2}$$

where,
n is the harmonic order,
V_n is the harmonic Voltage magnitude resulting from the harmonic current $\tilde{I}_n$,
I_n is the magnitude of harmonic currents in the line,
and ϕ_{in} and ϕ_{vn} are the phase angles of $\tilde{I}_n$ and $\tilde{V}_n$ respectively.

Impedance obtained using equation 2 may not represent the impedance of a supply. This is certainly true if loads generating harmonic currents are present in the AC supply system while testing, and if the transducers used to provide Voltage and current information are inadequate. Reliable measurement of an AC systems harmonic impedance in a non-invasive way is a difficult task requiring comprehensive investigation under a range of operating conditions, and the identification of all harmonic sources [15]. Clearly the CHART system

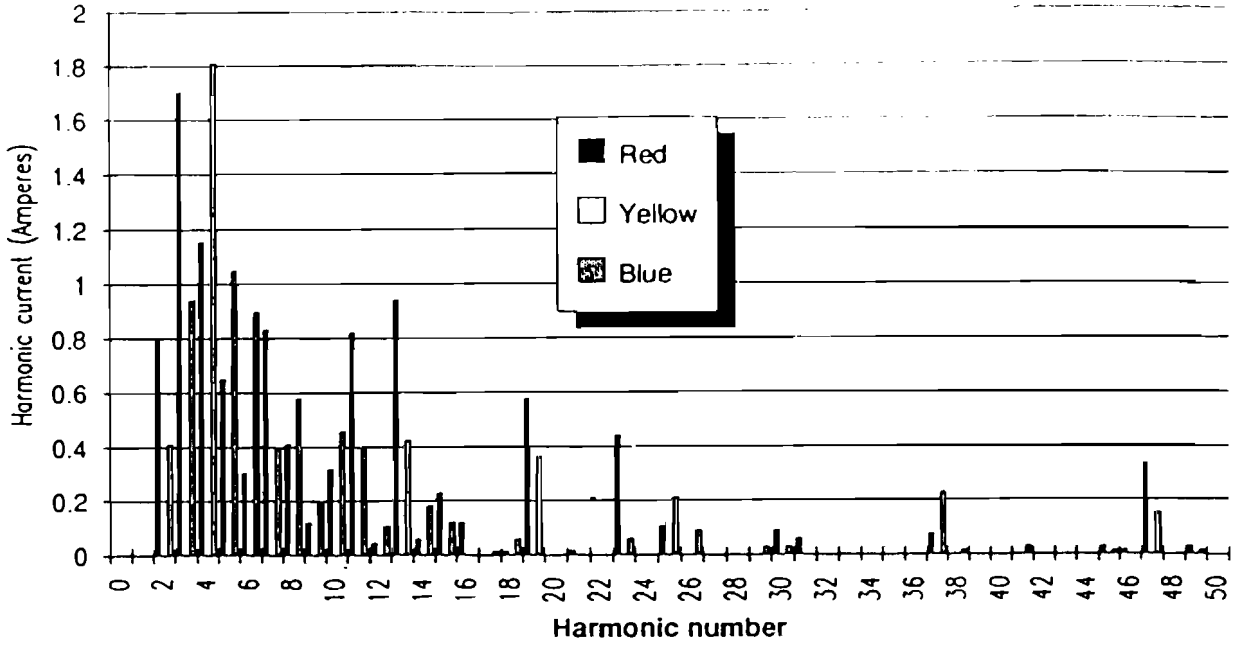

Figure 6: Harmonic currents measured at the Islington substation on the Islington-Twizel 220KV transmission line, 1:30pm, Wednesday July 25, 1990. Yellow phase current harmonics are not shown owing to problems with the fibre optic link.

is capable of calculating harmonic impedance, although the results require careful interpretation.

To be able to measure harmonic impedance makes CHART an extremely valuable tool in the comparison of actual harmonic impedance with theoretically determined harmonic impedance, and in harmonic filter design. When used to make measurements over a long time span, CHART can determine regions of harmonic impedance for three phases, rather than single points corresponding to harmonics on an impedance locus. Results from CHART are not confined to harmonic frequencies; by analysing Voltage and current over as many as 16 cycles, frequencies to an accuracy of almost 3Hz can be resolved.

Active and reactive harmonic power in each phase can also be obtained from harmonic Voltage and current, along with the direction in which they are flowing. This information could be useful in resolving harmonic problems by identifying sources of harmonic power. The direction of harmonic current flow can be used for this same purpose. Since accurate magnitude and phase information is necessary for this measurement, reliable CTs and VTs must be used - again the accuracy of CHARTs results is dependent on it being used correctly.

4 CONCLUSIONS

An advanced harmonic monitoring system has been described and its use in the field has been documented. The prime benefit of these tests has been to provide guidance on the future development of the CHART system.

Given the nature of the algorithms used to compute harmonic levels (namely the FFT) and the number of channels required, multiple digital signal processors (DSPs) are ideally suited to this application. The increased processing power afforded by DSPs can lead to simplifications in data acquisition hardware and an improved signal to noise ratio in the acquired signal by oversampling Voltage and current waveforms and filtering them using the DSP [16]. In addition to this, Multibus II in conjunction with Intel's multitasking real-time operating system (iRMX) forms a very powerful platform for multi-processing real-time systems. The tremendous number of features offered by the very highly integrated Multibus II CPU boards that Intel are now producing means that a Multibus II based system is even more attractive. At the beginning of 1991 the CHART II project team undertook to develop a Multibus II based DSP board using the TMS320C26 DSP. A successful breadboard of this was completed in May 1990, and has since been used as a software development platform for harmonic analysis software.

In parallel with developing software, a prototype Multibus II DSP data acquisition and processing module (DAPM) was designed and production of this began in September 1991. This is a two channel board incorporating a digital fibre optic interface to remote data conversion modules (RDCMs), two DSPs, and a full Multibus II interface. The full 20 slot Multibus II backplane can support up to 19 of these modules, with the Intel 486/133 Single Board Computer used to control and collect data from them. This means it is possible to configure a 38 channel harmonic monitoring system. The 486 computer also incorporates an Ethernet interface, enabling the connection of the CHART II system to a network. Control and display of the CHART II system is managed by applications written for Microsoft Windows 3.0 running on 386/486 PC workstations running MSDOS 4/5, which communicate with CHART II via Ethernet. The CHART II system is depicted in figure 7.

Conversion of analog signals representing Voltage and current to a 16 bit digital representation is performed in the switch yard by the RDCMs, and transmitted to the CHART II unit by fibre optic cable. Each channel uses an independent RDCM, which receives the sampling signal from the Digital Services Module (DSM) of CHART II, thereby ensuring that sampling occurs simultaneously on each channel. The DSM also accurately time stamps acquired data, with time obtained from the very accurate GPS satellite system.

The advantage of using RDCMs is that it dispenses with the need for an analog fibre optic system and the associated distortion resulting from its limited dy-

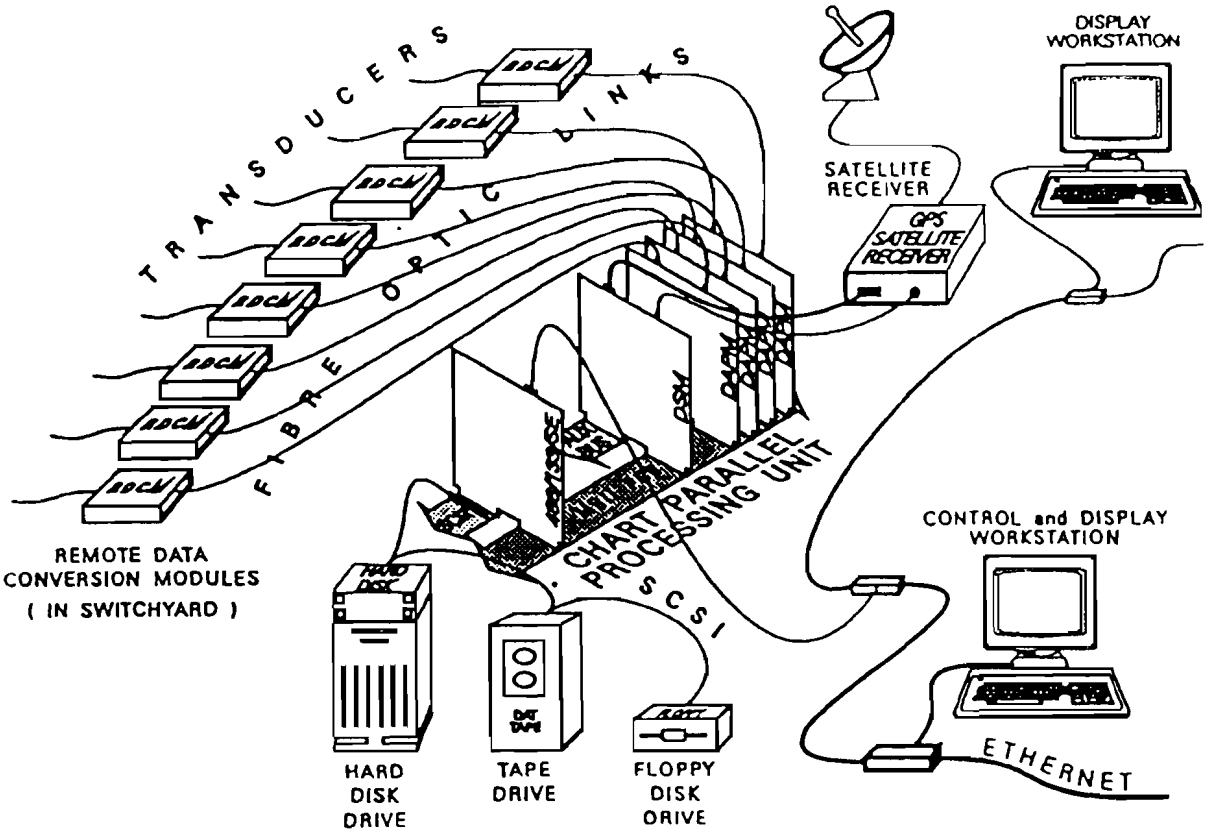

Figure 7: The CHART II harmonic monitoring system

namic range. It is therefore possible to accurately determine the fundamental component of Voltage and current as well as harmonic components. Additionally, the system is inherently more self contained and more easily calibrated. The increased processing power afforded by the DSPs means that a variety of algorithms can be used in harmonic analysis, ranging from finding harmonic components for every cycle of the fundamental, to up to 16 cycles of the fundamental. This allows accurate determination of harmonic components. The powerful 486 computer is capable of monitoring harmonic data on-line, and storing compacted data on a high capacity hard disk and DAT tape via its SCSI disk interface. It can also transmit data to the PC workstations via its ethernet interface for display. The use of Microsoft Windows 3.0 on the PC control and display workstations allows a variety of display types, ranging from bar charts of magnitude versus harmonic order, scratch graphs of magnitude versus time, and histograms of occurrence versus Voltage or current. It also enables harmonic data to be included into standard packages such as Microsoft Excel (a spread sheet package) for formatting into documents and subsequent processing. The system also has the potential for more sophisticated on-line

analysis algorithms to focus on specific results being sought and to reduce storage requirements.

Initial tests with the prototype CHART II unit will begin in the laboratory, examining harmonic levels produced by motor speed controllers using a set of specially constructed three phase CTs and VTs designed for use up to the 50th harmonic. This will enable fine tuning of the instrument before more extensive test are carried out on the New Zealand power system. During the commissioning of the upgraded New Zealand HVDC link, the system will be operated without the link in service. It is intended to measure harmonic levels during this time to determine background harmonic levels, and compare them with harmonic levels with the link in service. These tests are planned to be performed continuously for over one week to observe the effect of changing load conditions on harmonic levels. It is intended to present these harmonic levels over a long time span on histograms. Several peaks may occur on the histograms due to variations in operating conditions such as the DC link in service, shunt capacitors or synchronous condensers operating, and loads changing between industrial, commercial and domestic. These peaks can be labeled with their corresponding time and/or power system state.

ACKNOWLEDGEMENTS

The authors acknowledge the financial support of TRANSPOWER N.Z. LTD., and Allan Miller acknowledges the award of a 1989 UGC postgraduate scholarship. They also acknowledge the work of Charles Lake, Michael Cusdin and Michael Shurety who assisted in completing the CHART I prototype, and of Neil McKenzie of Design Power New Zealand who assisted in the field trials.

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A.5 Multi-Channel Continuous Harmonic Analysis in Real Time

92 WM 193-3 PWRD

Multichannel Continuous Harmonic Analysis in Real-Time

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Abstract - A flexible, modular multichannel continuous real-time harmonic analyzer with the capability of precision time stamping (via GPS satellite signals) of the acquired data is described. The key design features which provide this performance are fully discussed. These include remote distributed data conversion modules coupled via digital fibre optic links to parallel individual digital signal processor Multibus II based modules which are all controlled by a highly integrated 486 based module. The resultant Multibus II parallel processor system is run under the iRMXIII real-time operating system and is interfaced via ethernet to control and display workstations using a custom designed Windows 3 environment. The ready extension of the harmonic monitoring system to transient measurement is also described.

INTRODUCTION

The CHART system is designed primarily for the continuous analysis of power system harmonics in real-time. It has enough processing power to compute voltage and current harmonics for as many as 32 channels up to the 50th harmonic. Unlike known existing systems (PC based or dedicated instruments) which are only capable of short time span measurements, harmonics are computed for every fundamental cycle continuously and in real-time, and can be displayed as they occur. Furthermore, CHART can compute and display harmonic impedance and power at a busbar being monitored. The acronym CHART stands for continuous harmonic analysis in real-time, and the CHART system presented in this paper is a significant development of its predecessor, reported at the 1990 ICHIPS conference [1]. A powerful 486 computer, incorporating multiple coprocessors, is used to perform on-line monitoring of harmonic levels from selected channels to reduce the amount of storage and post processing required from monitoring. It does this by only storing relevant harmonic data to a hard disk for later retrieval. Relevant harmonic data might for example contain harmonics that have exceeded a predefined limit.

The CHART system is intended for use in a power station, substation, or laboratory. Hence it incorporates such features as independent data conversion modules, sited next to busgear and connected to the main CHART unit by fibre optic cables, and an Ethernet interface to facilitate connection of the unit to an existing network. The user interface to CHART is by means of custom designed application windows running under Microsoft Windows 3.0 on a 386/486 PC workstation running MSDOS 4.01/5.0, which is also connected to the network. This enables the workstation to be situated at a location other than that of the main CHART unit, and also enables multiple users to access CHART data by using different workstations. Multiple CHART units may be connected to the same network, and ethernet communication facilitates interconnecting to power system SCADA control systems.

CHART incorporates a GPS satellite time referenced accurate real-time clock feature that enables the unit to accurately time stamp data acquired from power system transducers. This feature, combined with CHARTs ability to sample voltage and current signals at frequencies higher than those required by harmonic analysis, means that CHART is a powerful tool for use in transient analysis of power system waveforms, and has found applications in fields such as fault location on transmission lines. Furthermore, by using several CHARTs at geographically separate locations on the same network, it has the inherent capability of enabling precise simultaneous measurement of power system parameters.

Other key features that make CHART a valuable research tool are its flexible sampling scheme, and its software development tools. CHARTs sampling scheme allows fixed sampling of waveforms at high rates for transient analysis, and coherent sampling at relatively low rates for harmonic analysis. Coherent sampling produces a set of equally spaced sam-

92 WM 193-3 PWRD A paper recommended and approved by the IEEE Power System Instrumentation & Measurements Committee of the IEEE Power Engineering Society for presentation at the IEEE/PES 1992 Winter Meeting, New York, New York, February 3, 1992. Manuscript submitted August 29, 1991; made available for printing November 20, 1991.

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ples that fit exactly into one period of the fundamental. Software for CHARTs front end DSP processors can be developed using development tools on its PC workstations and easily downloaded to the processors for execution.

This paper gives a general overview of the CHART system, covering topics such as its connection to current and voltage transformers on busgear , the parallel processing system and software used to compute harmonic levels , and the networked user interface to the system.

AN OVERVIEW OF CHART

The CHART system is illustrated in figure 1. It consists of three main sections: The Multiple Remote Data Conversion Modules (RDCMs), a parallel processing system, and a network of workstations.

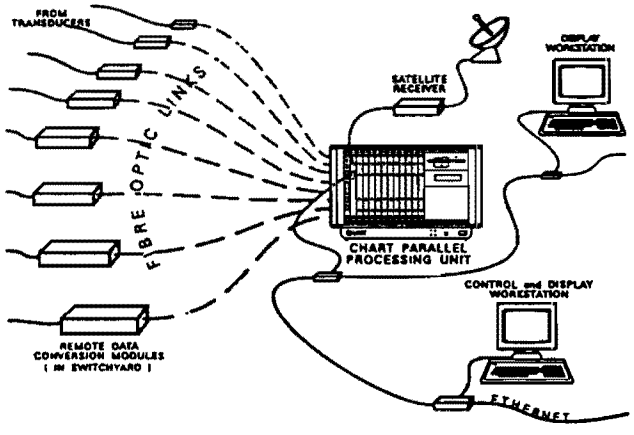

Figure 1: The CHART harmonic monitoring system.

As depicted in figure 1, each analog voltage signal, representing either voltage or current, is converted to a digital representation by the Remote Data Conversion Modules (RDCMs) and transmitted to the CHART parallel processing system by fibre optic cable. This isolates the CHART computer equipment and users from potentially hazardous voltages developed under fault conditions in a switch yard. The fibre optic cables can be replaced with normal wire cable in the laboratory. The use of optical links between the conversion modules and the processing system eliminates the problem of ground loops in the instrumentation system.

The CHART parallel processing system is responsible for the computation of harmonic levels in the signals received from the RDCMs, and for monitoring the levels. It also handles communication of data to display workstations. The configuration of the CHART parallel processing system, and the display of harmonic levels, is handled by PC workstations running microsoft Windows. The CHART system and the workstations are networked on Ethernet, which is used to communicate data between CHART and the workstations.

Remote Data Conversion Modules

The remote data conversion modules are used to convert current transformer and voltage transformer outputs to 16 bit digital signals, and to transmit them to the CHART processing system. The RDCMs are typically located next to busgear (either interior or exterior), near the current and voltage transducers to which they are connected. They receive their analog to digital conversion command from the CHART parallel processing system, thereby ensuring that conversion occurs simultaneously on each channel. Sampling is synchronous with the power system fundamental. In a specific application, consideration must be given to propagation delays in the fibre optic links if sampled data is to be time stamped accurately. Each RDCM is a stand-alone module, powered independently by batteries, trickle charged by a solar panel, which avoids the running of power leads between units in a monitoring environment, and which also enables a high degree of freedom of placement of the modules when connecting CHART to a power system. Alternatively the RDCM units can be powered by a common supply. This in turn enables a large amount of flexibility in monitoring various points on a power system. Separating the RDCMs from the main processing unit facilitates the tailoring of the analog/digital conversion circuitry to particular application requirements in a functional and cost effective way.

The structure of a typical RDCM is outlined in figure 2.

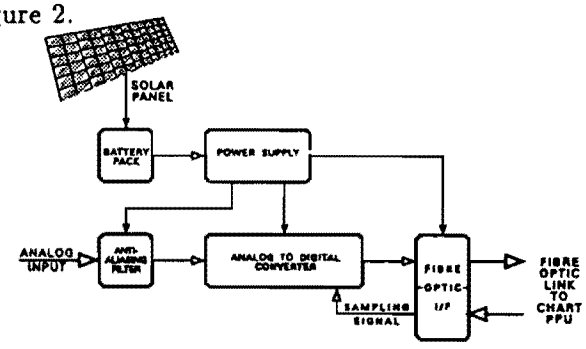

Figure 2: A remote data conversion module.

The CHART Parallel Processing System

The CHART parallel processing system is based on the Intel Multibus II bus architecture and uses the Intel Real-Time Multitasking operating system (iRMX) to schedule the tasks required to collect, monitor, and distribute data. Harmonic levels in the signals acquired from the RDCMs are computed using fast Fourier transforms (FFTs) [2], which is a computationally intensive process. For this reason, processing in the CHART system has been distributed over multiple processor cards and moved as close as practicable to the front end data acquisition stage. The general structure of this is illustrated in figure 3.

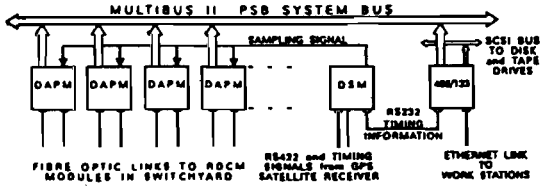

Figure 3: The CHART parallel processing unit.

Multiple Data Acquisition and Processing cards or Modules (DAPMs) are arranged to acquire and process two channels of data each, giving a total of 2n channels (where n is the number of DAPMs). These cards incorporate a full interface to the Multibus II parallel system bus (iPSB), and are capable of message passing their results to any other card on the bus. However, as illustrated in figure 4, the system software is arranged so that the 486/133 card acts as a central collection point for the DAPM results, and also performs any further computation required. If the computation required is too great for the 486/133 card, it can "farm" computation out to other processor cards added at a later stage as the system expands. This illustrates the importance of a good multiprocessing bus - one of the advantages of Multibus II is that extra processor cards can be added with minimal effort.

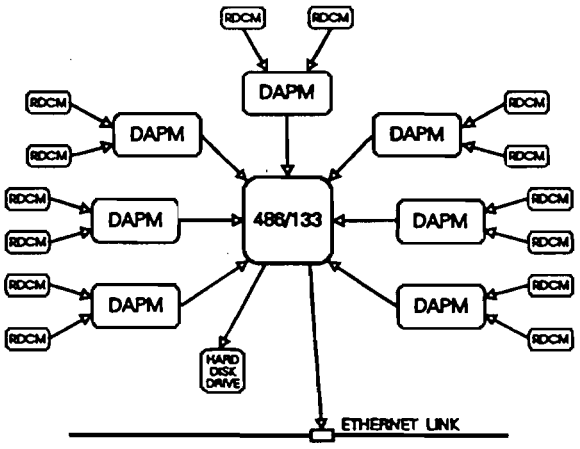

Figure 4: Data flow in the CHART parallel processing system. The 486 computer acts as a central collection point for DAPM data.

The final card in the central processing system is the Digital Services Module (DSM) whose functions are twofold. Firstly it provides accurate timing and fundamental frequency information to the 486/133 card for time-stamping of acquired data, and secondly, it produces sampling and synchronisation signals for the data acquisition stage. The DSM monitors the power system fundamental frequency and produces a sampling signal that is exactly 1024 times the frequency of the fundamental [1]. Sampling of voltage and current is therefore coherent, and spectral leakage [2] from the FFT is minimal. Because spectral leakage is minimised by coherent sampling, the added computational burden of windowing the input data is not required. The DSM can also produce a sampling signal of fixed frequency if selected by a user, and can produce a sampling signal of 102.4/112.88 KHz for transient analysis of 50/60 Hz systems. A GPS satellite receiver interface is incorporated into the DSM to enable it to receive very accurate timing information. This time is latched by the sampling signal and matched with captured data by the 486 computer. The DSM communicates timing data to the 486 through a spare serial port on the 486. Even higher sampling rates are possible (in the order of 1MHz) with the appropriate RDCM design.

The maximum number of channels that can be monitored by the CHART system is limited by three factors. Firstly the number of available slots on the Multibus II backplane, secondly the extra processing power required to process the extra data, and finally limitations of the iPSB bus bandwidth. The largest Multibus II backplane has 20 slots, and with one 486/133, 19 are left free for DAPMs. The extra processing requirements for harmonic analysis are added to the system automatically as more channels are added, in the form of DAPMs, which perform the FFT processing. The only other processing required is for monitoring of harmonic levels computed by the DAPMs. Depending on the complexity of the monitoring required, one 486/133 may be powerful enough to perform this. The iPSB bus can support a sustained transfer rate of 10 Million transfers per second. When configured for harmonic analysis, the combined transfer rate for 19 DAPMs is less than 1 Million transfers per second. Bus bandwidth and processing power would however be limiting factors with the significantly higher sampling rates used by transient analysis.

Data Acquisition and Processing Modules

Each DAPM incorporates a fibre optic cable interface, and can acquire raw time domain data (in a serial digital format) transmitted from two independent RDCMs. As depicted in figure 5, two Texas Instruments digital signal processors (one for each channel) are used to process the acquired data. The DSP results are stored in "first in first out" (FIFO) buffers for message passing to the 486/133 card by the direct memory access (DMA) unit in the 80186 microcomputer. The 80186 microcomputer handles all message transactions over the Multibus II parallel system bus (PSB) via the bus interface unit. The DAPM card also supports interconnect space - a feature of Multibus II that allows centralized control

and coordination of all cards identification, configuration , and diagnostics [3].

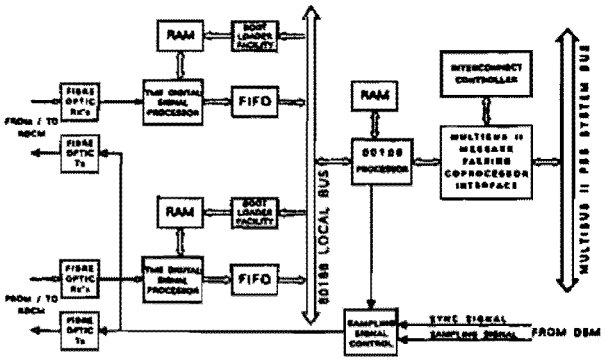

Figure 5: Data acquisition and processing module structure.

Each DSP has 64Kwords of external static RAM, divided into 32Kwords of program RAM and 32K words of data RAM. This amount of external data RAM enables the DSPs to buffer data when sampling at higher sampling rates for transient analysis. A DMA facility from the 80186 microcomputer to the DSPs program RAM is provided. Hence an image of a program that a DSP is required to execute can be placed directly into its program RAM by the host 80186. Software operating on the 80186 is able to receive this program image over the PSB from the 486/133 computer. The 486 originally received it from a workstation, via ethernet, where it was developed using the DSP software development tools. When instructed by the 486/133, the host 80186 can boot the DSPs to begin their program execution. The ability to download bootable program images to the DSPs from a workstation is a key feature of CHART, giving it tremendous potential as a research tool, as well as a power system instrument. Using this feature, CHART can be used for a variety of functions such as harmonic analysis over any number of cycles of the fundamental, or fault detection. The analysis technique used is selected by the user at a workstation from a number of options. The appropriate bootable image is then downloaded to the appropriate DSP, taken from a collection of pre-compiled DSP programs corresponding to each option.

For harmonic analysis, voltage and current waveforms are sampled at eight times the frequency required to resolve up to the 50th harmonic. Oversampling in this manner reduces the complexity of antialiasing filters in the RDCMs and leads to an improved signal to noise ratio in the sampled signal. The sampling signal is generated on the DSM and sent via each DAPM to the RDCMs. The DAPM can gate the sampling signal to each RDCM independently if data from that channel is not required. A data flow diagram illustrating the data flow rates and processing performed by a DSP for harmonic analysis is shown in figure 6. Acquired data is passed through an 8:1 decimation antialiasing finite impulse response (FIR) filter [4]. This reduces its rate to precisely 128 samples per 50 or 60 Hz cycle. The FIR filter output is placed in a FIFO buffer as well as being passed to an FFT routine. This performs an FFT over data accumulated for 1, 2, 4, 8, or 16 cycles, depending on which analysis program was selected by the user, and places the output data in a second FIFO buffer. Obviously for the DSP to perform FFTs continuously on a cycle by cycle basis, data must be buffered, which is another reason for the DSPs external data RAM.

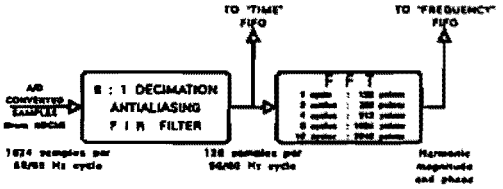

Figure 6: Data flow and processing for harmonic analysis.

The 486 computer

As discussed previously, the CHART processing system software is arranged so that the 486/133 single board computer acts as a central collection point for the data from all of the DAPMs. The 486/133SE card is a highly integrated Intel single board computer that incorporates an 80486 microprocessor with internal cache RAM and coprocessor operating at 33MHz, 16Mbytes of dynamic RAM, a full Multibus II interface, a SCSI protocol controller for interfacing to disks, a DMA controller, several serial I/O controllers, and a LAN coprocessor for interfacing to Ethernet. This computer acts as a compute server, monitoring harmonic levels received from DAPMs and computing harmonic power and impedance, a disk server, storing and retrieving harmonic data, and a communication server, interfacing the processing system to workstations on Ethernet.

The principle behind the operation of this board is that only data required "down stream" for further processing is obtained from a DAPM. Hence the Multibus II resources are not tied up handling unwanted data. Each DAPM can be viewed as a data server, supplying four separate types of data (for harmonic analysis). These four data types are:

•Time domain data from DAPM channel A
•Frequency domain data from DAPM channel A
•Time domain data from DAPM channel B
•Frequency domain data from DAPM channel B

Multiple DAPMs provide an array of data for the multiple channels, with each data type uniquely addressable over Multibus II.

If a particular type of data is required by some task operating on the 486 computer (a communication task to a workstation for instance), a requesting task for that data is created and attached to the address of the data. It then requests the data, and when received from the DAPM (in the form of a standard packet) sends copies of it to other tasks via mailboxes. Any task requiring the data must create a mailbox for receiving the data, and catalogue it with the requesting task. This data flow between tasks is illustrated in figure 7.

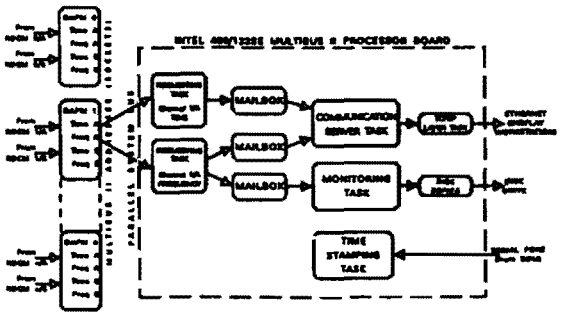

Figure 7: An example of multiple tasks operating on the 486 computer.

The 486/133 computer runs the iRMX operating system which schedules the various tasks. The 486 also handles bootloading of the DAPM software during the boot phase of the system operation [5], and incorporates Multibus II central service functions that provide system level services to all of the DAPMs [3].

CHART Control and Display Workstations

The display of power system voltage and current waveforms and of harmonic data is accomplished with custom designed application windows running under Microsoft Windows 3.0 on 386/486 PC workstations running MSDOS 4.01/5.0. The various data types are displayed on windows which are selected using a mouse and icons. Windows can be moved about the screen and scaled to any desired size. Multiple windows can also be displayed, with data in each window updated approximately twice a second. Various displays are possible, such as magnitude versus harmonic number, voltage (per unit) and current (Amps) versus time, and magnitude for particular harmonics versus time. Figure 8 shows a typical harmonic display from CHART. The harmonics displayed in the window are actual levels measured during field testing of a prototype CHART unit at a New Zealand substation. The fundamental is not shown to enable appropriate scaling of the harmonics. The display shown is a black and white copy of a colour screen. The benefit of viewing the harmonics using a colour monitor is that each channel is distinguishable by colour - in this case red, yellow, and blue.

Ethernet is used as the physical communication path between display workstations and the CHART parallel processing unit. The protocol TCP/IP is used as the software layer on Ethernet, providing the CHART unit with a suite of standard applications such as FTP and TELNET. Actual harmonic data and time domain waveforms that are to be displayed are sent from the parallel processing unit to display workstations using TCP/IP sockets. Only one workstation in the network environment can modify CHART parameters - the control and display workstation. Telnet is used by this workstation to remotely log a user into the parallel processing unit (server). The user can then configure the CHART system for monitoring. This involves: naming channels; entering system parameters such as the nominal voltage, current and voltage transformer ratios, and the system frequency (50 or 60 Hz); selecting the sampling source (fixed or synchronized to the fundamental); and selecting the method of harmonic analysis (essentially whether the FFT should be computed over 1, 2, 4, 8, or 16 cycles). An example of the main display terminal on the control and display workstation is shown in figure 9. Display workstations essentially have read only access to chart data. Users at these workstations can view CHART data, but cannot modify CHART settings.

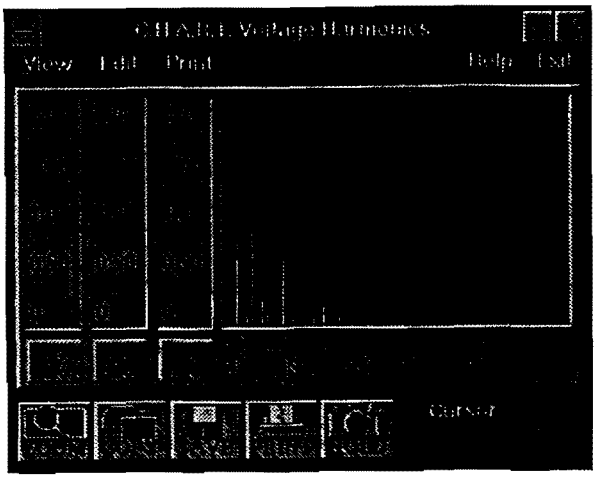

Figure 8: Voltage harmonics for three phases displayed on the CHART user interface. The harmonics are shown as a percentage of the 220KV nominal system voltage.

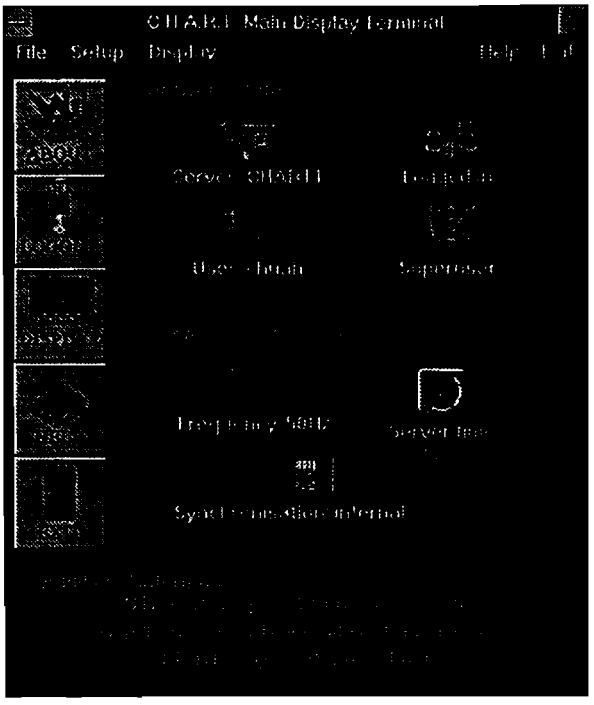

Figure 9: The main display terminal on the control and display workstation. The user Chuah has remotely logged into the CHART server.

CONCLUSION

A very advanced data acquisition and parallel processing system aimed specifically at continuous real-time power system signal monitoring has been described. The need for the system arose initially from the desire of Transpower N.Z. Ltd., who supported the project, to accurately monitor the presence of power system harmonics on the New Zealand national grid [6]. The system described here is the latest version to evolve from the research activities over the last 5 years of the Power Systems Group at the University of Canterbury into power harmonic measurement. It is significantly different from earlier versions reported on in [1] and [5] and provides a precision time referenced measurement capability which has hitherto not been possible.

The key features of the system which distinguish it from other data acquisition systems (usually PC based) or instruments which are capable of measuring harmonics are embodied in the system acronym CHART. Continuous measurement indicates that there is no break in the acquisition and processing of source data thus ensuring the integrity of the measured signals. Real-time capability provides the facility to observe the processed results as they occur. The on-line analysis of the processed data effectively enables efficient monitoring, analysis and storage of power system harmonic information - experience has shown that this in itself can be a major impediment to properly policing harmonic pollution. The multichannel modular nature of the system means that it can be tailored to a wide range of power system monitoring configurations. Furthermore the ethernet network facility enables it to be readily integrated into existing SCADA system controllers and to be accessed by any number of workstations. Another key feature of the system is the remote analog to digital data conversion at the transducer end with a digital fibre optic interface which minimises noise and earth loop problems while ensuring maximum signal bandwidth, resolution and integrity. Finally the incorporation of a highly accurate widely accessible time reference by the use of the GPS satellite signals provides the system with the unique capability of being able to time stamp acquired data to within 1 microsecond. This last feature will, by employing multiple independent systems, provide simultaneous power measurements across a complete transmission power grid with a timing precision that has not been possible before.

The design details described in this paper identify the important technical considerations in providing the performance and flexibility sought in such a monitoring system. The choice of bus architecture, bus bandwidth, true multiprocessing capability and the real time operating system are key elements in the design of a flexible and powerful parallel processor measurement system. The inherent flexibility of the system with its time stamping facility also enable the application to be extended to transient measurements which find ready application in, for example, HVdc fault location. The system is presently being fully tested in the laboratory environment and is scheduled for field trials on the New Zealand grid in the latter half of 1991. On-going development of the on-line analysis programmes and enhancements to the control and display workstations software will continue into 1992.

ACKNOWLEDGEMENT

The authors acknowledge the financial support of TRANSPOWER N.Z. LTD., and A.J.V. Miller acknowledges the award of a 1989 UGC postgraduate scholarship. They also acknowledge their colleagues Khoo Hiang, for assisting in the development of digital signal processing software, Dennis Chuah, for his work with Microsoft Windows 3.0, TCP/IP, and software installation, Malcom Barth, for assisting in design work, Dermot Sallis, for his technical assistance, and Jos Arrillaga for his enthusiasm and general support.

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A.6 Multi-Channel Real Time Harmonic Analysis using Multibus II

MULTI-CHANNEL REAL TIME HARMONIC ANALYSIS USING THE INTEL MULTIBUS II BUS ARCHITECTURE

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Abstract

Legislation sets limits for harmonic levels on electrical power systems and provides the requirement specifications for harmonic measuring equipment. This paper describes an instrument developed to measure harmonic levels continuously in real-time and to assist in the resolution of harmonic problems. The instrument is based on the Intel Multibus II bus architecture, and uses three Intel single board computers, operating in parallel, to achieve continuous real-time harmonic analysis. The computationally intensive algorithms required to perform harmonic analysis are realized in this instrument by operating two of the boards in a stand alone mode (they are not running an operating system). The software development for these boards is discussed in detail. This includes: the ability to load programs into a boards RAM over the PSB from an RMX board and execute them, message passing software to enable the transfer of large amounts of data over the PSB and to enable the transfer of general control messages, queue structures to buffer the tasks running on each board, and acquisition software to acquire data from a custom built data acquisition system over an SBX bus. The queues on each board are shared by multiple tasks, which must have mutually exclusive access to the queues to avoid corruption of data in them. The actual harmonic analysis application software (averaging and FFT algorithms for the stand alone boards) is also discussed, with particular emphasis on methods used to increase its execution speed. The final single board computer in this instrument runs the RMX II.4 operating system. The multiple tasks running on this board include the collection of data from the stand alone boards, the compaction and storage of this data to a mass storage device, and the transmission of harmonic data to a PC-AT for display via a general purpose interface bus (GPIB) connected to the boards SBX bus. All of the software for the Intel single board computers is written in either PL/M-86, ASM86 or PL/M-286.

The paper discusses the use of this instrument in the field, based on field tests recently carried out, and finally the future development of the instrument using the Intel Multibus II bus architecture is discussed. This is likely to involve the modification and transfer of the software to an Intel 520 system. It is expected that each board in this system will run the RMX operating system, greatly simplifying the implementation of multiple tasks and message passing, and that the display of harmonic data will be achieved using the Intel real time graphics interface, or software running on a Multibus II PC subsystem.

Abbreviations used

Table 1 lists the abbreviations and their meanings used in this paper.

PIC programmable interrupt controller
PIT programmable interval timer
MPC message passing coprocessor
SCC serial communications controller
DMA direct memory access
CPU central processor unit
CSM Central services module
SBC single board computer
PSB parallel system bus
SBX system bus extension
LBX local bus extension
RAM random access memory
EPROM erasable programmable read only memory
CS code segment
KB Kilobyte
MB Megabyte
GB Gigabyte
FFT fast Fourier transform
DFT discrete Fourier transform
ASM86 Assembler 86
PL/M86 Programming language M 86
RS232 serial communication protocol
GPIB General purpose interface bus
BIST built in self test
SDM System debug monitor
OEM Other equipment manufacturer
RSVP répondez s'il vous plaît [French: please reply]
DSP Digital signal processor

Table 1: Abbreviations

1 INTRODUCTION

An harmonic monitor is essential to police the harmonic pollution created by electricity consumers and it must comply with legislative requirements if the results of the monitoring are to be used in any legal proceedings. New Zealand legislation provides the requirement specifications for harmonic measuring equipment [1]. The following main requirements were derived from the legislation [2].

- Measure the harmonic levels of six AC voltage and current waveforms up to the 50^{th} harmonic, giving amplitude information.
- Input sampling should be synchronized to the power system fundamental component .
- The harmonic processor should process a sampled time domain signal consisting of 4, 5 or 6 consecutive cycles. These may be averaged to one cycle for processing.
- Should sample all six channels simultaneously.
- The analyzer should sample as near continuously as possible.
- Local display of at least one channel's spectrum or a display of one harmonic on all 6 channels. The display should also show the fundamental frequency and whether this is within the limits for harmonic monitoring set in the legislation.
- Magnetic tape storage on a minute by minute basis.
- Hard copy records of user selected results.

A research group in the Electrical and Electronic Engineering department of the University of Canterbury has, over the last four years, been developing an instrument that complies with these specifications. In April 1990 a prototype of the instrument was completed, which has since been used in field tests to monitor harmonic levels at various points on the New Zealand power system.

Other features such as the calculation and display of harmonic power and impedance, and the acquisition of an extra two channels (giving a total of eight input channels) were included in the design, and with these, the instrument is not only useful in assessing legislative compliance, but is also a valuable tool for ongoing research into power system harmonics.

The harmonic monitor uses the Multibus II bus architecture for it's processing requirements. A custom built data acquisition system acquires eight analogue signals obtained from power system current and voltage transformers, and handles the task of locking the sampling frequency to the power system fundamental frequency (for either 50Hz or 60Hz power systems). The data is processed by the Multibus II processors, and harmonic data are displayed using an IBM compatible PC/AT. The harmonic monitor is illustrated in Figure 1.

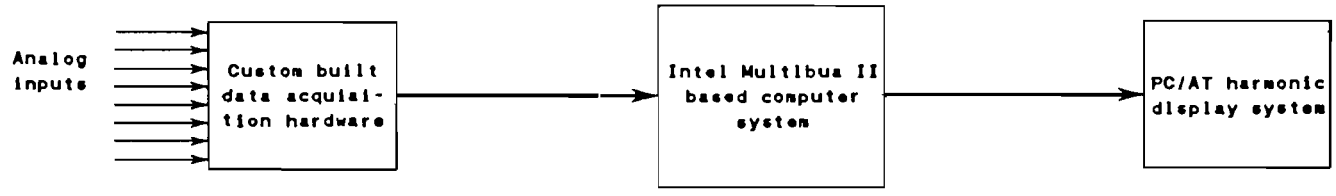

Figure 1: The harmonic monitor

In 1985 Intel's Multibus II was adopted as the bus standard for the parallel processing requirements of this instrument. These include data acquisition, FFT processing, storage and display. This decision was made because Multibus II was considered technically superior to other bus standards, and with Intel's backing it was expected to become a widely accepted standard. With this acceptance we expected a range of Multibus II OEM products to become available. These included DSP processors, data acquisition boards and graphic cards. Unfortunately these did not emerge with the speed expected, which significantly slowed the projects progress.

The system configuration of the present harmonic monitor is illustrated in Figure 2. Data is acquired over the SBX bus and averaged by the 186/110 prototyping board. This board runs as a stand alone board (it does not run an operating system) primarily to achieve high speed processing, and is controlled by messages from the master CPU (the iSBC 286/100A). The prototyping board was used to avoid developing a complete data acquisition CPU board with a Multibus II interface. The software running on this board is discussed in Section 2. This includes the data acquisition and averaging software, and bootstrapping the board to execute a bootstrap loading program after a reset or when the board is powered up.

Averaged data from the 186 board is message passed to the iSBC 386/120 board for FFT analysis. Originally the RTI-980 array processor board was intended to be used to compute the FFT of the averaged data, however when problems with it's availability were experienced, a 20MHz 386 board was used. Again this board runs as a stand alone board (it does not run an operating system) to achieve high speed processing. The software development for this board is discussed in Section 3. This includes the development of bootstrap loading programs, serial communications, and message passing software. The application software running on the 386 board is discussed in Section 4.

Harmonic data from the 386 board are message passed to the iSBC 286/100A board, which runs multiple tasks such as collecting data from the stand alone boards, controlling the stand alone boards, compaction and storage of harmonic data to the 40MB Winchester hard disk, and the transmission of harmonic data to the PC/AT for display via a GPIB bus connected to the boards SBX bus. This boards runs the RMX II.4 operating system which handles the multiple tasks in real time as well as providing system calls for message passing and disk access, which speed up the application software development. The 286 board software is discussed briefly in Section 5.

2MB of off board memory is provided by the MEM/320 board via the LBX bus, and the iSBC 186/224A multi-peripheral controller provides access to various types of mass storage media. These are: a 40MB Winchester disk, a 360KB floppy disk, and a quarter-inch 60MB streaming tape used for system backups and data archiving.

Both the stand alone boards are configured so that their software executes in RAM, which is faster than executing in EPROM as it is not necessary to insert wait states. Down-loading software was developed for both the boards. This enables a program to be loaded into a board's RAM, over the PSB from the RMX board, and executed. The development of this down-loading software is discussed in Section 3.3.

The 386 board is operated in the real mode which allows the 80386 CPU to support the same programming

model as the 8086. It therefore supports the execution of 8086 programs. This enables the portability of software between the 186 and 386 boards. The code for these boards is written in PL/M86 and ASM86. All code for the 286 RMX board is written in either PL/M286 or ASM286.

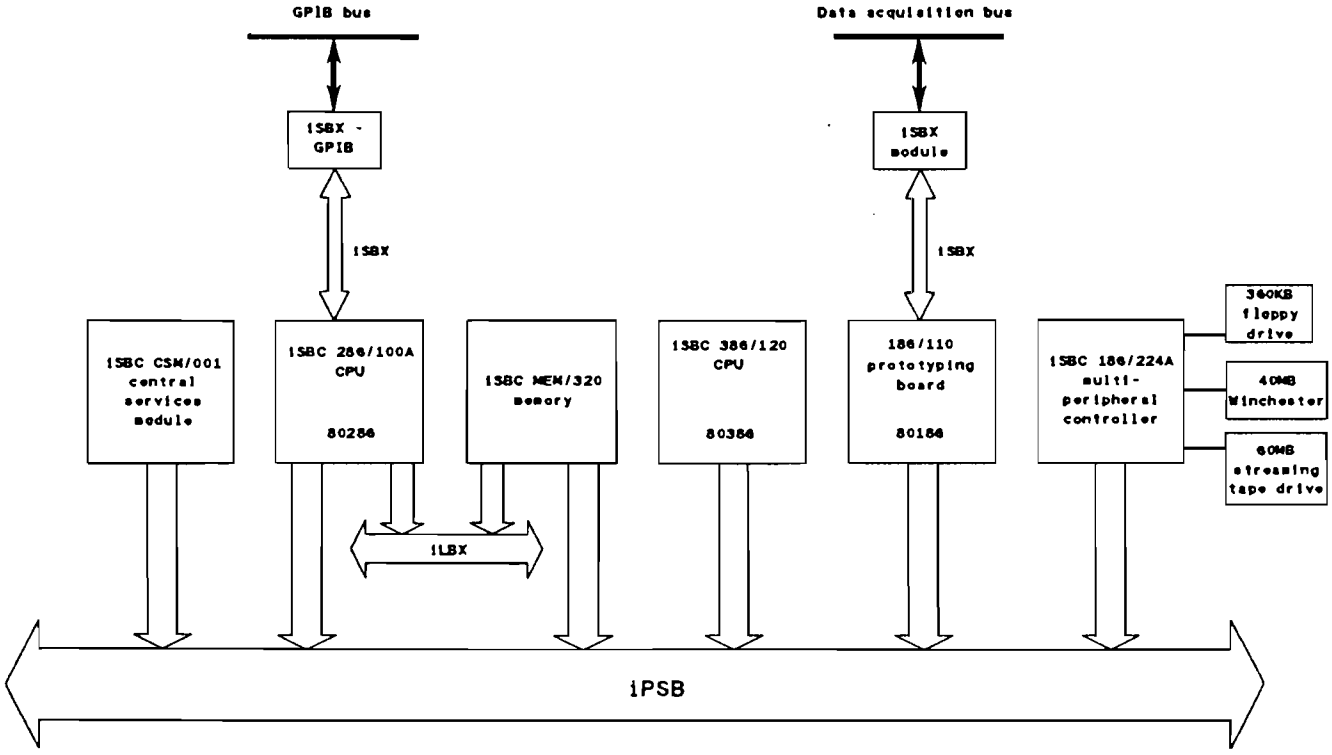

Figure 2: Harmonic monitor system configuration

2 186/110 PROTOTYPING BOARD SOFTWARE

The prototyping board performs four main tasks. These are: the acquisition of data over the SBX bus from the data acquisition system, the averaging of 4, 5 or 6 cycles of data, the message passing of data to the 386 board, and the control of the data acquisition hardware (primarily the automatic control of front end gain devices). These tasks are illustrated in Figure 3. Averaging is performed to reduce the amount of data and to enhance the periodic (harmonic) components in the acquired signal [3] [4].

The input buffer of Figure 3 is shared by three tasks which run concurrently and which therefore must have mutually exclusive access to the data in the buffer. Mutual exclusion was achieved by setting up a circular buffer of 4, 5 or 6 blocks, corresponding to the number of cycles to be averaged, illustrated in Figure 4(a). Data consisting of one cycle of the power system fundamental is transferred to each block consecutively. When full, a block is released to the averaging task which takes the data from the block and adds it to an average data packet. The block is then reserved for data acquisition again (using flags). When 4, 5 or 6 blocks have been acquired and averaged, the average data packet is added to the output queue. This occurs when the processor is free from acquiring and averaging.

The data acquisition task is interrupt driven and therefore has a higher priority than the remaining three tasks, which essentially have equal priority. Because the process of data acquisition, averaging and message passing is unique (each task occurs at one particular time for a constant time), they run in a set order and task scheduling does not present a problem.

The data acquisition and averaging tasks (discussed in Section 2.1) are the most CPU intensive, with each requiring approximately 20 percent of the available time to run. The software is set up so that these run continuously, and when the CPU is free, the message passing and hardware control tasks run. Message passing requires only a small amount of CPU time, as it is mainly performed by the MPC and the DMA controller.

The averaging task essentially follows the acquisition task around the input buffer as depicted in Figure 4(a).

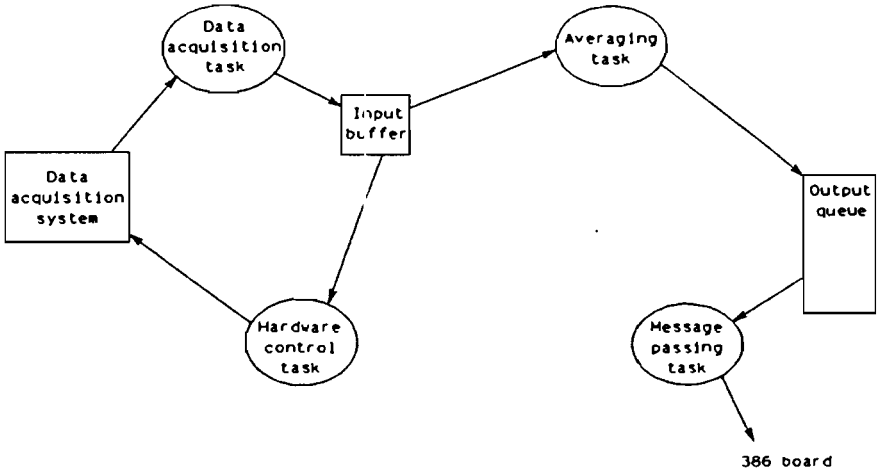

Figure 3: Multiple tasks running on the 186 board.

2.1 The Data Acquisition and Averaging Tasks

To read each sample from the data acquisition hardware after each analog to digital conversion is too slow, as there is a large overhead involved in setting up the hardware and reading one sample from the analog to digital converter output. Burst transfers enable more efficient data transfer. These are performed by repeating primitive operations in hardware. PL/M86 provides a call (blockinword) that does this, enabling very fast data transfer over the SBX bus. To make a burst transfer possible, the data acquisition hardware incorporates a FIFO buffer which interrupts the 186 board's CPU when it contains one cycle of data. The CPU then transfers one cycle (128 samples x 8 channels = 1024 samples) into the input buffer. This is illustrated in Figure 4(b). Ultimately DMA will be used to transfer data from the data acquisition FIFO buffer into the 186 board's memory, freeing the CPU for other tasks.

The data averaging task involves adding one block of data to another, without dividing through by the number of blocks added, as this ensures that the time domain data is scaled to produce accurate results from the FFT algorithm, discussed in Section 4.2.

The averaging routine was written in assembler where primitive string operations are set up and repeated in hardware, producing code that executes extremely rapidly.

2.2 Bootstrapping the 186 Board

The BIST test handler in the 186/110 board's EPROMs looks at the address FFFF 0008h in the BIST EPROMs for a pointer to a BIST customization structure (BCS) [8]. The BCS can be used to execute software automatically after executing the BISTs.

A BCS was written in ASM86 and linked with a PSB hexadecimal down-loading program (discussed in Section 3.3). It was then located at the start of EPROM. The BCS address was programmed into location FFFF 0008h of the BIST EPROMs. The BCS points to the start of the 186 board PSB hexadecimal down-loading program, which is executed after the BISTs following a reset or when the board is powered up, allowing code to be loaded into the 186 board's RAM from the 286 board.

3 iSBC 386/120 BOARD SOFTWARE DEVELOPMENT

This section discusses the development of software for the stand alone 386 board. The discussion includes bootstrapping the 386 board (Section 3.1), the development of serial communication with the board (Section 3.2), and the development of down-loading software to load code directly into the 386 board's RAM. This was achieved in two stages: firstly down-loading via the serial port, and secondly, down-loading over the PSB from an RMX board. Both stages are discussed in Section 3.3. Finally the development of solicited message passing is discussed in Section 3.4. This section also discusses general concepts involved in solicited data transfers.

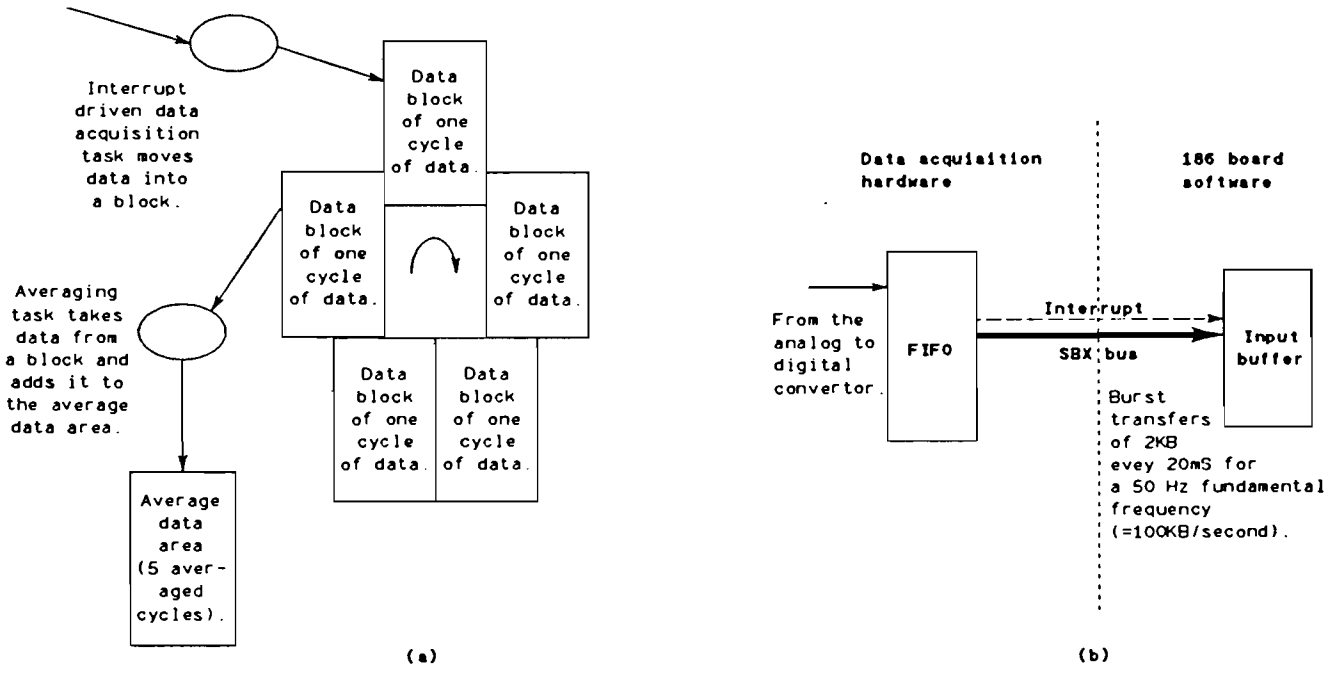

Figure 4: (a) The circular input buffer arrangement showing the averaging task following the data acquisition task for 5 cycle averaging. (b) The data acquisition system FIFO arrangement to allow burst transfers of data over the SBX bus

3.1 Bootstrapping the 386 Board

The 386 board's BIST EPROMs are located in the top 128KB of the 4GB CPU address space, as shown in the memory map of Figure 5. To enable the 386 board to execute code after running the BISTs a program table [10] was made in ASM86 and located at FFFF FF20 using a locator. This table contains the start address of the program (user code) that is to run after the BISTs.

Initially a bootstrap program was written and combined with the program table. This was located in the top 64KB of EPROM as shown in Figure 6(a) at FFFF 0000h. This program is pointed to by the program table and therefore runs after the BISTs. The bootstrap program is written in ASM86 and copies the top 64KB of EPROM into the top 64KB of RAM and executes, in RAM, the application software which was also located in the top 64KB of EPROM, above the bootstrap program at FFFF 0100h as shown in Figure 6(a). The application software executes rapidly in RAM compared to EPROM as wait states are not inserted.

The program table and bootstrap program were located using the locator and Intel hexadecimal code was generated from the located code. This code was merged with the original BISTs (using a specially written hexadecimal code merging program) and with the actual application program (written in PL/M86, located above the bootstrap program and converted to hexadecimal code) to produce the final EPROM contents, depicted in Figure 6(a), which was then programmed into the EPROMs. This process is illustrated in Figure 6(b).

The bootstrap program essentially establishes code in the lowest 1MB of memory (RAM) before executing it by executing a long jump.

3.2 Implementing Serial Communications With the 386 Board

After writing the necessary bootstrap code to establish and execute application code in RAM, the application code itself was written.

To begin with, a program enabling communication with the iSBC386/120 board via a terminal using the RS232 port was written. This required programming the 8751 SCC and 8259 PIC hardware devices on the board to build up high level calls. These were programmed during the initialization stage of the application program. Initialization of software and of hardware devices on the board is essential for it to function correctly.

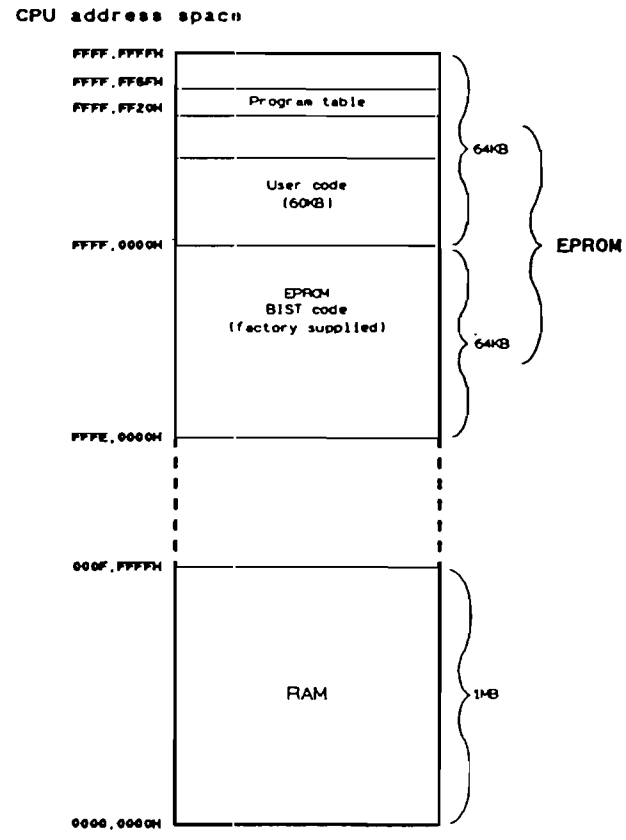

Figure 5: The 386 Board Memory Map.

Communication is achieved by reading and writing from or to the interconnect space and character input is achieved using an interrupt handler. The RS232 interrupt vector was set to point to the interrupt handler routine during initialization.

The resultant module provided high level calls such as those shown in table 2.

```
call write$string(@(19,'This is an example',CR,LF));
char = get$char;
```

Table 2: PL/M86 serial communication calls.

The application program was compiled, linked with object modules, located at FFFF 0100h, and converted to Intel hexadecimal format. Linking was performed to combine all object modules and the resulting relocatable object module was located to an absolute object module and converted to hexadecimal format for programming into the EPROMs.

The program development cycle used to develop programs for the 386 board is shown in Figure 7.

After a program's source code has been written, it is compiled, linked, located, and converted to Intel hexadecimal format. As described in Section 3.1, it is merged with the BISTs and the bootstrap program and loaded into EPROMs. The EPROMs are then placed into the 386 board which is then powered up and the program tested. If it does not operate satisfactorily, the source code is modified and the process of compiling and programming EPROMs is repeated until it is satisfactory. A typical program may require several iterations round the modify loop, and because EPROMs must be erased and reprogrammed each time, it can take a considerably long time to develop a simple program.

3.3 Development of Down-loading Software

The delay involved in each iteration can be significantly reduced by loading a program directly into RAM rather than programming EPROMs. A program was written that used the serial communication procedures described in Section 3.2 to load a program via the 386 boards's serial port, from another computer, into RAM. The software running on the board then comprised the bootstrap program running in EPROM which establishes and executes a bootstrap loader in RAM. This bootstrap loader then waits for Intel hexadecimal records from

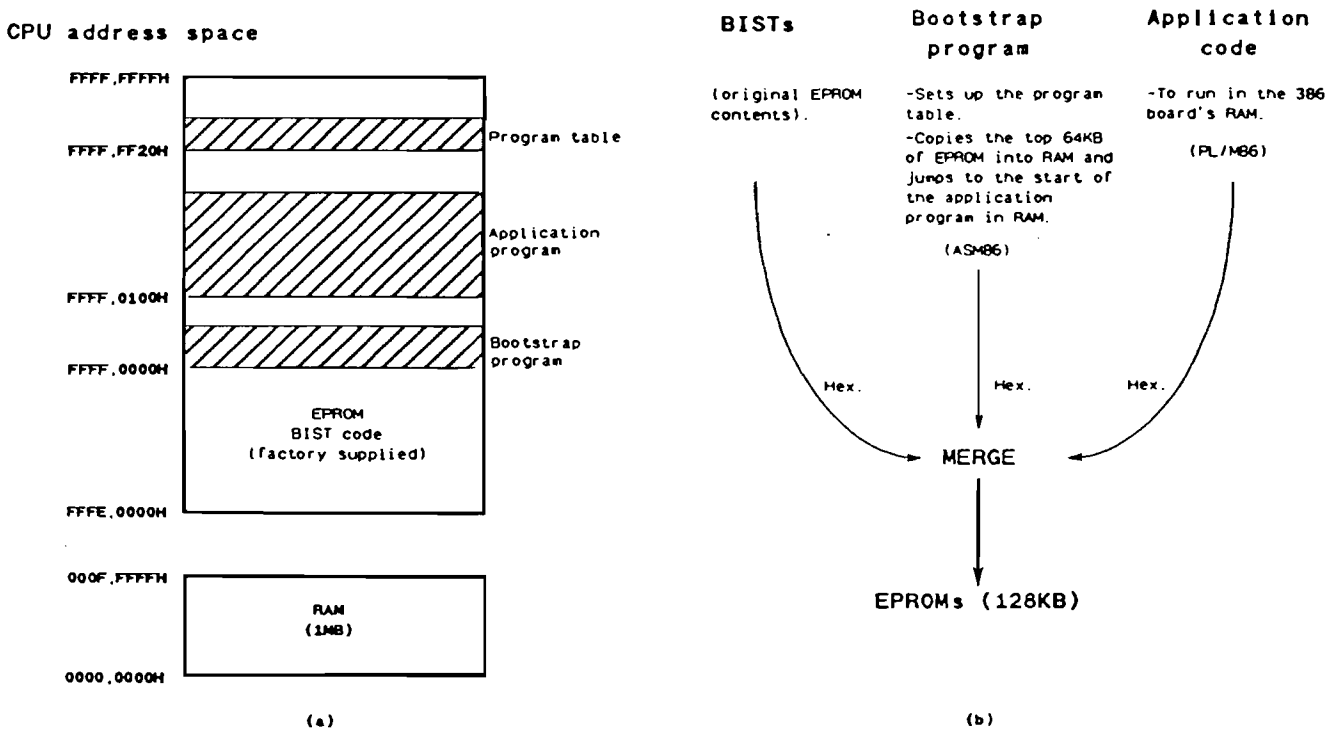

Figure 6: (a) Memory map showing the EPROM contents after programming. (b) The process of merging the various code to produce the final EPROM contents.

the board's serial port, which it decodes, placing data (from data records) at the appropriate address, noting the codes start address (from the start address record), and beginning program execution when it encounters an end of file record.

The hardware configuration for this is illustrated in Figure 8(a), with the software flow illustrated in Figure 8(b). Figure 8(c) shows the resulting memory map at the completion of 8(b). This process reduces the delay indicated in Figure 7, circumventing the tedious programming of EPROMs.

With the decreased program development time, unsolicited message passing over the PSB was developed. This required the programming of the MPC and PICs which was implemented in a module which provided high level calls to send and receive unsolicited messages.

Using the unsolicited massage passing ability, the serial hexadecimal down-loading program was modified to load programs over the PSB from the iSBC286/100A board which runs RMX286 II.4. A program was written to execute on the 286 board which read the hexadecimal code from the hard disk and passed it to the 386 board using unsolicited messages.

This PSB hexadecimal down-loading software was extended to the 186/110 prototyping board (linking to the 186 boards object modules - because of different hardware) to enable loading of code from disk into the 186 boards RAM also. This reduced the delay indicated in Figure 7 to approximately one minute, significantly improving the software development capabilities of the system. At power up each board is reset by the 286 board, which loads the appropriate software into each board's RAM from harddisk, or the user can reset and load code to either board when required.

3.4 Development of Solicited Message Passing for the Transfer of Large Amounts of Data Over the PSB

Solicited messages enable the transfer of large amounts of data between boards over the PSB. RSVP solicited messages [11] are used which require buffer negotiation using unsolicited messages as illustrated in Figure 9(b). The actual message passing is implemented in a message passing module separate to the application software, thereby hiding the mechanics of message passing from the application. This is illustrated by the layered model

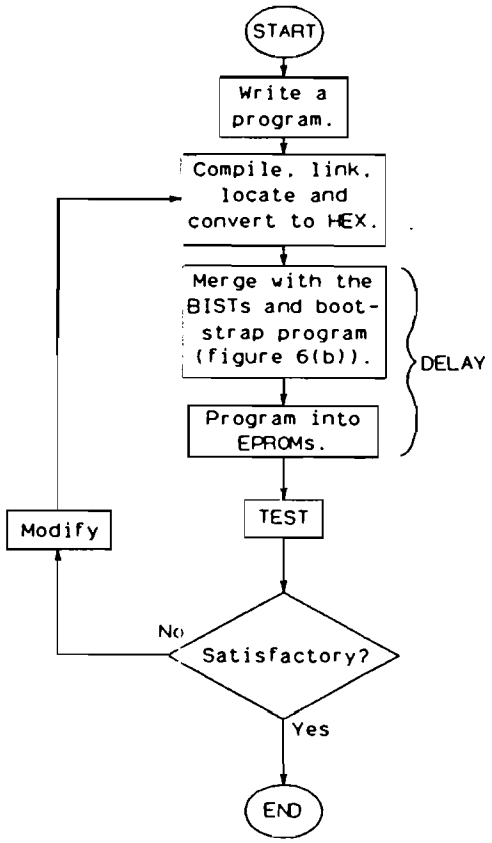

Figure 7: The program development cycle

shown in Figure 9(a). The message passing module sits below the application code. If, for example, the application running on the 186 board wants to send data to the 386 board, it calls the necessary routine in the message passing module, which in turn programs the DMA controller and sends and receives the necessary unsolicited messages involved in a solicited transfer using the MPC (and a data link protocol). The messages are received by the 386 board's MPC and interrupt the processor. An MPC interrupt handler in the message passing module decodes the messages, eventually making the received data available to the application running on the 386 board.

Figure 9(b) illustrates an RSVP solicited message transfer. A transfer is initiated by the board requiring data sending an RSVP request unsolicited message to the sending board. This interrupts the sending board which decodes the RSVP request. If it has data to send, it programs it's DMA controller to send the data and sends a buffer request unsolicited message to the receiving board. Otherwise it stores the RSVP request until it has data to send. The buffer request interrupts the receiving board, and if it has sufficient memory available to receive the data it sets up it's DMA controller to receive the data and sends a buffer grant unsolicited message to the sending board. If it does not have sufficient memory available, it sends a buffer reject unsolicited message. The buffer grant is not seen by the transport layer on the sending board, but automatically begins the data transfer between the memories of each board using their respective DMA controllers. On the last transfer, the processor of each board is interrupted, indicating that the solicited data transfer is complete.

4 386 BOARD FFT SOFTWARE

4.1 Multiple Tasks on the 386 Board

The 386 board performs two main tasks. Firstly, the computation of the DFT of one averaged cycle of data for six channels using an FFT algorithm as discussed in Section 4.2, and secondly, message passing tasks to send and receive data. Time domain data representing one averaged cycle of each input channel is received as

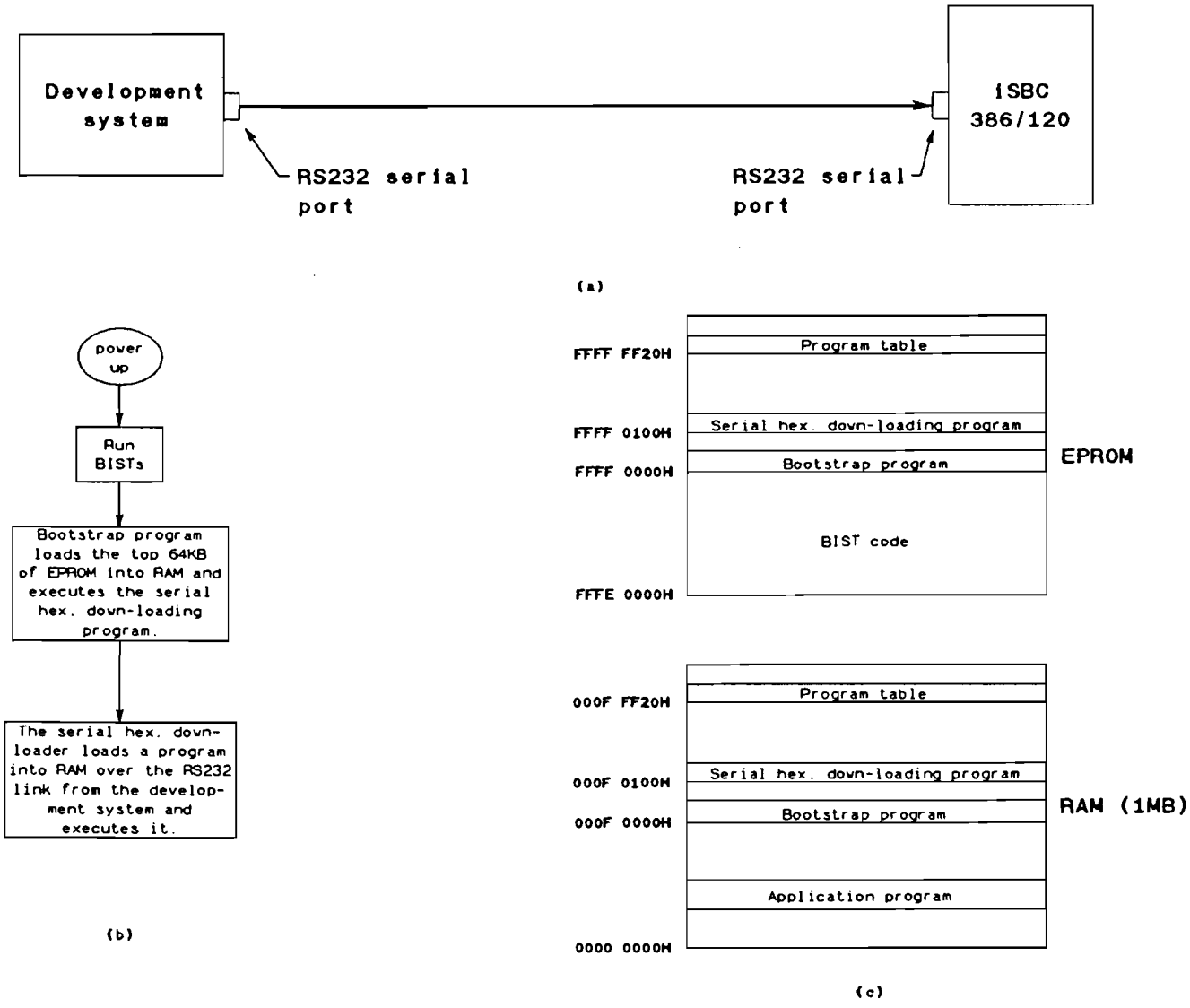

Figure 8: (a) Serial down-loading hardware configuration, (b) Serial down-loading software steps, (c) Resulting memory map after serial down-loading.

a packet from the 186 board. The FFT of this is then computed and the resulting frequency domain packet is sent to the 286 board.

Queues were set up to buffer the FFT tasks and to buffer the message passing tasks sending and receiving data. Because these multiple tasks run concurrently and share data in the queues, their access to the data must be mutually exclusive. Mutual exclusion was achieved by designing the task structure around the RSVP solicited message transfer and using flags to control access to queues. This is obviously inflexible, although to build up an elaborate scheme for mutual exclusion would be equivalent to building part of an operating system which would add unnecessary processing overhead and software development time.

Figure 10(a) depicts the solicited message passing arrangement between the three main processor boards in the harmonic monitor. Time domain data is acquired by the 186 board and passed to the 386 board using RSVP solicited messages. This computes the FFT and sends the resulting frequency domain data to the 286 board, also using RSVP solicited messages (discussed in Section 3.4). The queues and FFT algorithm on the 386 board were structured as shown in Figure 10(b).

The 386 board application software begins the message passing process by sending an RSVP to the 186 board, which eventually replies with the buffer request $(b)_i$. The 386 board then reserves room in it's time domain (input) queue, sets up it's DMA controller for data input and sends a buffer grant to the 186 board. If it's time domain queue is full, it sends a buffer reject. The buffer grant ((c)) initiates the data transfer, and

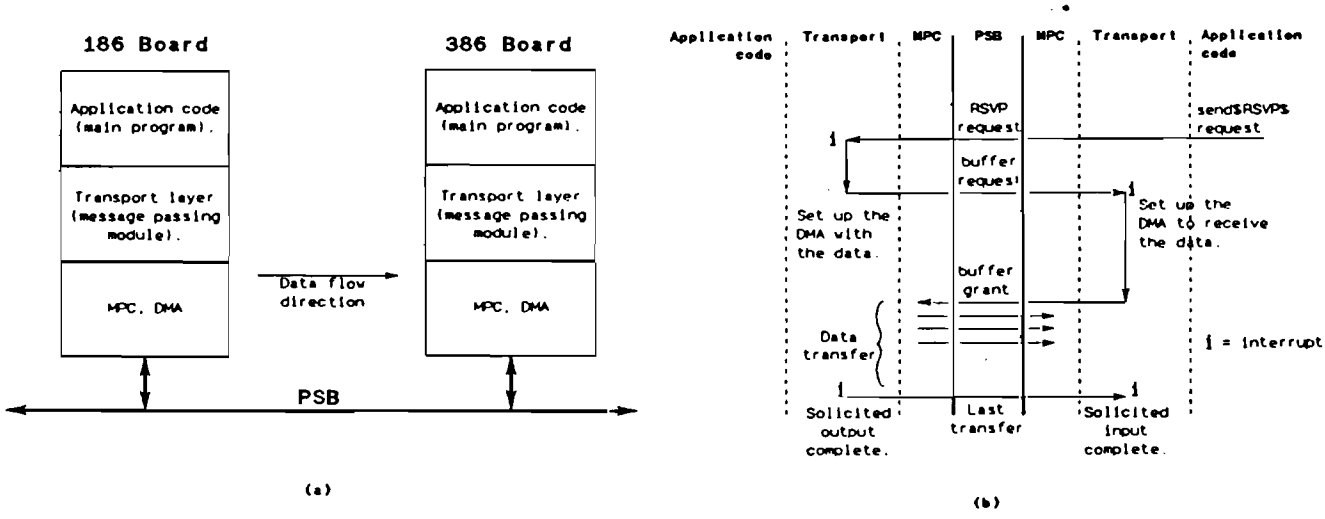

Figure 9: (a) A model representing the layered message passing system. (b) Messages involved in a solicited message transfer.

when this has completed (indicated by the interrupt $(c)_i$), the time domain queue input pointer is updated and another RSVP is sent to the 186 board.

Data is removed from the time domain queue independently of data arriving in it. The application program obtains a pointer to the data in the queue output but does not update the queue output until the FFT of this data has been computed and the result added to the frequency domain (output) queue. If an entry is removed from a full queue, an RSVP is sent to the 186 board to obtain more time domain data.

When the 386 board receives an RSVP request from the 286 board (indicated by the interrupt $(1)_i$), it responds with a buffer request and sets up its DMA controller, with data from the frequency domain queue output, for data output. If the frequency domain queue is empty, it stores the RSVP request and waits until data is added to the queue before sending a buffer request and setting up it's DMA controller. A buffer grant ((3)) sent from the 286 board initiates the data transfer. The interrupt $(3)_i$ indicates that the data transfer is complete, and the frequency domain queue output pointer is updated.

The actual FFT algorithm is discussed in the following section (Section 4.2).

4.2 The FFT Algorithm

A 128 point radix-2 FFT algorithm [5] [6] is used to find the DFT of each cycle of data. This is followed by routines which compute the magnitude and phase of the complex output data and which compensate the magnitude and phase results to account for the non-uniform frequency responses of power system transducers [3].

The algorithm was originally implemented using floating point arithmetic, although this was too slow for this real-time application. The algorithm was then modified to use fixed point (integer) arithmetic, using registers as much as possible and avoiding reference to memory. This improved the codes execution speed significantly. Look up tables were also used to improve execution speed and the code was hand optimized in assembler (ASM86), resulting in an algorithm fast enough for this application. Timing tests of the FFT algorithm operating on the 20MHz 386 board with the overhead of message passing show that the board can compute the FFTs of six channels in approximately 50 percent of the available time.

The input time domain data to the FFT algorithm is represented by integers, requiring 16-bit representation. The multiplication of two of these integers can possibly result in an overflow. To avoid this problem, the most significant 16-bits of the 32-bit result (from a 16-bit by 16-bit multiply) were taken as the multiplication result. This requires that the input data be scaled to occupy the full 16-bits if precise results are required.

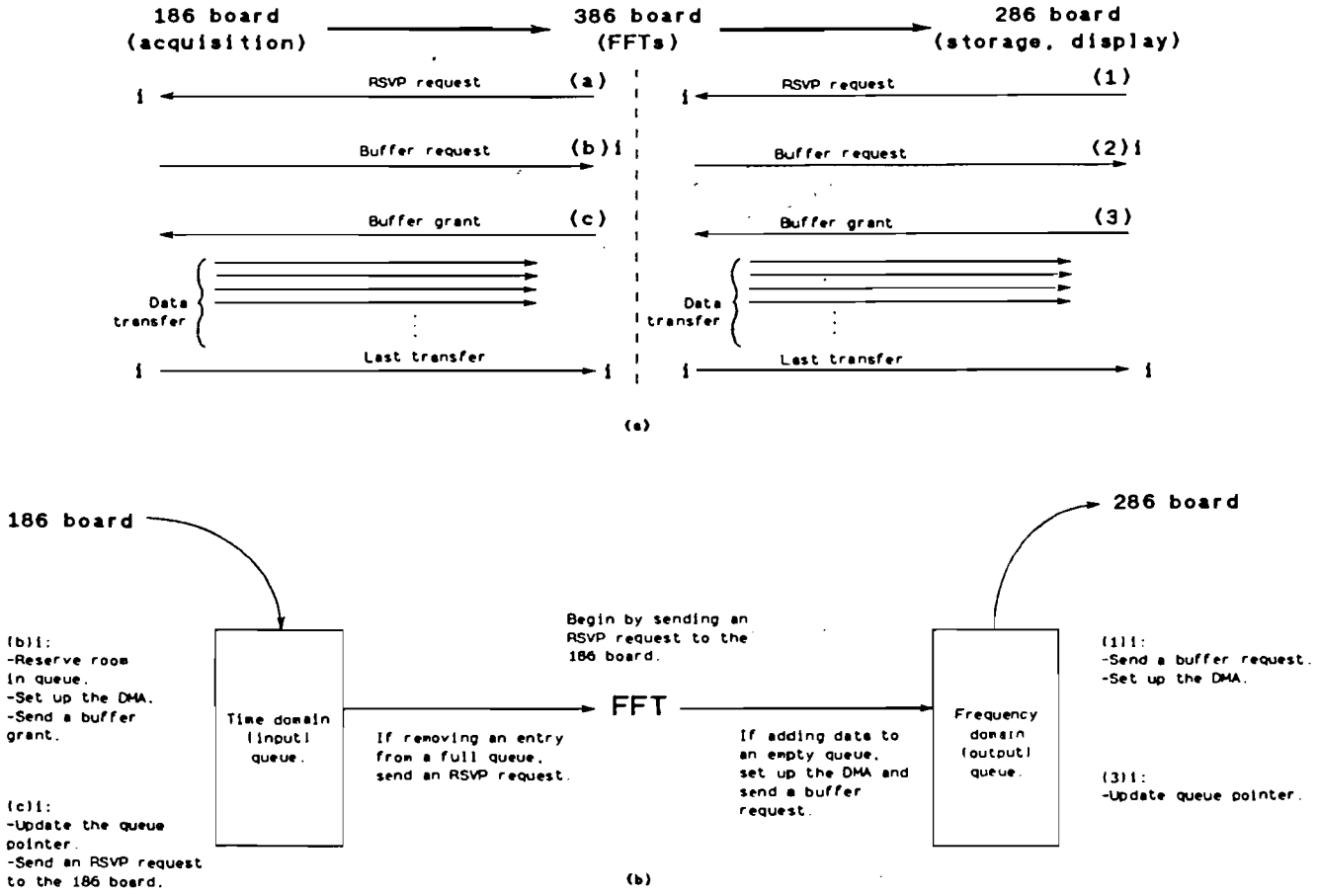

Figure 10: (a) Solicited message passing, (b) 386 board Queue and FFT algorithm structure.

5 iSBC 286/100A BOARD SOFTWARE

The 286 board runs the RMX II.4 operating system. This allocates CPU time to multiple tasks running on the board, enabling the system to operate in real-time. The main tasks involve the collection of harmonic data from the 386 board using RSVP solicited messages, discussed in Sections 3.4 and 4.1, compacting the harmonic data and storing it on the hard disk, the transmission of the data to the PC/AT for display, and handling exceptions from the stand alone 186 and 386 boards. The software running on this board also sends a configuration message to the 386 board containing tables for compensation of harmonic data, discussed in section 4.2, and sends start-up messages to both stand alone boards to begin data acquisition and analysis.

6 CONCLUSION

A working prototype of the instrument, completed in April 1990, has since been used in field tests conducted at a New Zealand substation and further field tests are planned for the end of the year. The initial test was more a logistical exercise rather than one to perform a specific measurement to resolve an harmonic problem. Results from the instrument were compared with results from other harmonic analysers and were found to be the same. A considerable amount of harmonic data was also stored for analysis in the laboratory, although an important feature in future developments of the instrument will be on-line analysis to avoid collecting and analysing data at a later time.

Programming boards without an operating system required a lot of work and consequently the software development was slow. This is not practical for a commercial product, but provided an interesting educational exercise in this case, giving an appreciation of the RMX operating system - particularly in the areas of Multibus

II message passing and real-time multi-tasking.

The next stage in the development of the instrument will be the modification and transfer of the software to an Intel 520 system. The processing requirements will be met by three 386 based single board computers, with each board running the RMX operating system. This will simplify the writing of software to run multiple tasks on each board, and the system calls provided by RMX will allow a more flexible design. The data will still be acquired over an SBX bus from the custom built data acquisition system, although DMA transfer will be used to free the CPU for other tasks.

Initially the Intel real time graphics interface was to be used as the display for harmonic data, however the use of the Multibus II PC subsystem with a Multibus II interface has also been investigated. The commercial analysis package ASYST will be added to this PC board to allow flexible design of the user interface.

The possibility of building a DSP based harmonic analyser with a DSP in the front end of each data acquisition channel is also being examined.

ACKNOWLEDGEMENT

The authors are grateful of the financial support offered by the Electricity Corporation of New Zealand and the Power Systems Group of the Electrical Engineering Department for the development of this instrument. A.J.V. Miller acknowledges the award of a University Grants Committee postgraduate scholarship and of a Transpower New Zealand postgraduate scholarship.

Mr. C.B. Lake assisted in the development of software for the stand alone Multibus II boards, and also assisted with project management. His work was of tremendous value. A significant contribution to software development for all Multibus II boards was made by Mr. N.R. Hadfield who was one of the first students involved with the project. Mr. M. Shurety has also contributed significantly with his work on the software for the 286 RMX board. We thank Mr. M.J. Cusdin for handling communication with Intel and for obtaining information on the various Multibus II products.

Project leadership and direction was given primarily by Mr. M.B. Dewe, and the authors acknowledge the interest of Professor J. Arrillaga.

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A.7 HAIP Harmonic Measurement Field Test

HAIP HARMONIC MEASUREMENT FIELD TEST

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August 1990

Abstract

The harmonic measurement field test conducted using the HAIP harmonic monitoring instrument during July of 1990 is reported. The test showed that the HAIP harmonic monitor can be moved from the laboratory to the field and used to make harmonic measurements when interfaced to a power system using Design Power's fibre optical measuring system. Issues concerning correcting for the fibre optical measuring system's highly non-uniform frequency response are discussed in detail, and it is shown that this measuring system introduces a large error into the fundamental component, making reliable measurement of the fundamental almost impossible. Relations relating results from the HAIP harmonic monitor to actual power system voltage and current are developed and preliminary results from the test are presented. The future development of the instrument based on features relevant to this test is summarised. The Islington end of the Islington to Twizel transmission line was monitored throughout the test.

Contents

1 INTRODUCTION

This document reports the results of the harmonic measurement field test conducted at the Islington substation between July 23 and 26, 1990. The harmonic measurement equipment (hereinafter referred to as the *harmonic monitor*) developed by the Electrical and Electronic Engineering department of the University of Canterbury under the Harmonic Analysis and Instrumentation Project (HAIP) [1], [2], [3], [4] was used in the test.

The test was primarily a logistical exercise to demonstrate that the harmonic monitor can be moved from the laboratory environment to the field and used to make harmonic measurements. Associated with the logistical exercise was the need to show that the harmonic monitor can be connected to Design Power's fibre optical measuring system to produce valid results. This was achieved by comparing the harmonic monitor's results with Design Power's existing harmonic measuring equipment (3 NOWA-1s controlled by a PC/AT). The configuration of the harmonic monitoring equipment and its connection to the fibre optical measuring system is detailed in Section 2, with a discussion of the fibre optical measuring system given in Section 3. Moreover, the test provided the first opportunity to relate the harmonic monitor output to actual power system voltages and currents. The development of relations relating observed results from the monitor display to power system voltages and currents is given in Section 4.

The emphasis of this document is not on presenting actual harmonic levels with their subsequent analysis from the system monitored, but rather discusses the practical issues concerned with moving the harmonic monitor to a substation or power station, connecting it to the power system, and using it to produce meaningful results. A considerable amount of harmonic data was stored while monitoring and the analysis of this data is currently underway in the Electrical and Electronic Engineering Department. Preliminary results from the field test are presented in Section 5. Section 6 discusses the future development of the harmonic monitor, based on the experience gained from this field test.

The Islington substation was considered a suitable location to conduct the initial field test because of its proximity to Canterbury University and because it has a 220KV bus with lines linking major South Island generation points and loads as illustrated in Figure 1. It's 220KV bus is also linked via Twizel to Benmore which, because of it's converters, is a source of harmonics. The Islington to Twizel line was monitored throughout the test primarily for protection reasons - the circuits from Islington to Twizel through Tekapo B and Bromley maintain system security in the event of harmonic monitoring equipment causing protection to operate on the Islington to Twizel line.

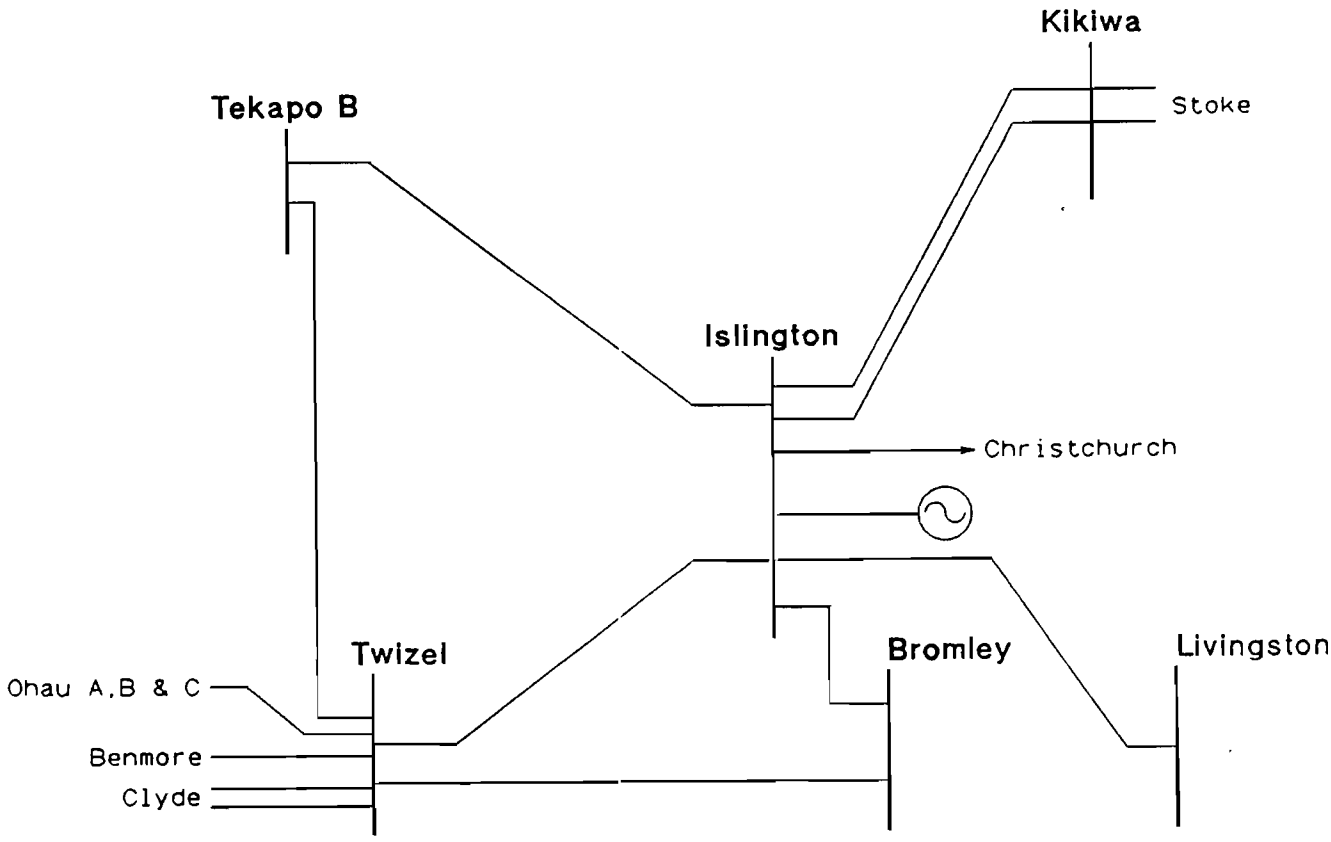


Figure 1: Single line diagram showing the location of Islington substation in the South Island Power System.

2 SYSTEM CONFIGURATION

The current transformer (CT) and voltage transformer (VT) connections to the Islington to Twizel line are shown in Figure 2. Existing magnetic CTs were used to measure the line currents of all three phases and capacitor VTs (CVTs) were used to measure the voltage of each phase of the 220KV line. The CTs used have a reasonably 'flat' frequency response across the range of interest (from 50Hz to 2500Hz), although the CVTs used have unknown non-linear frequency responses, rendering any results unsuitable for rigorous analysis [5], [6], [7]. However, because the analysis of harmonics was not the primary consideration, as explained in Section 1, these VTs were suitable for this test. The Design Power special purpose capacitive divider VTs normally used for harmonic measurements were not available as they were not functional at the time of testing.

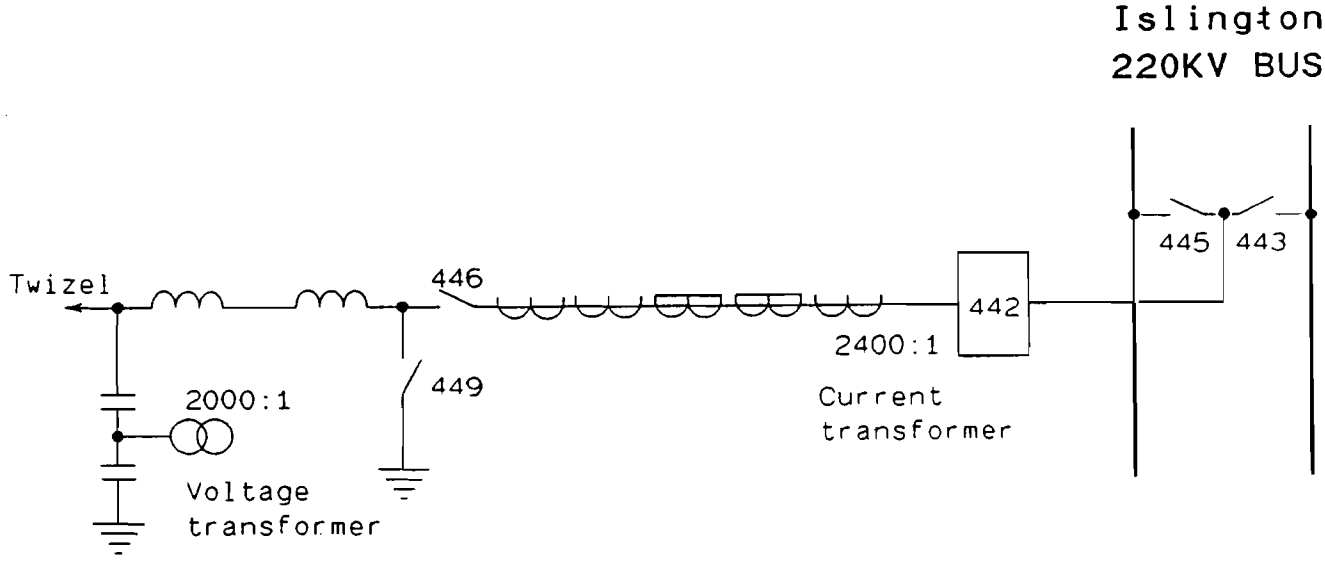


Figure 2: Current transformer (CT) and voltage transformer (VT) connections

The voltage signals obtained from the CTs and VTs were transmitted to the harmonic measuring equipment as illustrated in Figure 3. Design Power's fibre optical measuring system consists of the filters, fibre optical cables, and buffers. The filters (together with fibre optic transmitters) are housed in two steel filter cabinets situated next to the measurement points in the switchyard as shown in Figures 4 to 6.

Each filter cabinet is supplied with power from distribution outlets situated in the switchyard. The filters and the fibre optical transmission equipment are discussed further in Section 3.

The fibre optical cables were run from the monitoring site where the harmonic monitors were sited (the relay room next to the control room) through existing ducting to the measurement points in the switchyard. Figure 7 shows the harmonic monitoring instrumentation located in the relay room. On the left is the Design Power equipment consisting of 3 NOWA-1 harmonic analysers controlled by a PC/AT, with the HAIP harmonic monitor on the centre right. This consists of the data acquisition system, the Multibus II based computer system, and the PC/AT [1], [2], [3]. The fibre optical receivers and buffers are situated between the two harmonic monitoring systems. The orange cables connected to the receivers and buffers are the fibre optical cables, which are stored on the reels visible in the bottom of the photograph. The outputs of the buffers are connected to both the Design Power NOWA-1s and the HAIP harmonic monitor, using single ended connections and BNC connectors, to facilitate a comparison of the two systems.

To satisfy New Zealand harmonic legislation [8], [9], the power system voltage and current signals must be sampled coherently [1], [2], [3], [10], [11], [12], which, because the filters dramatically attenuate

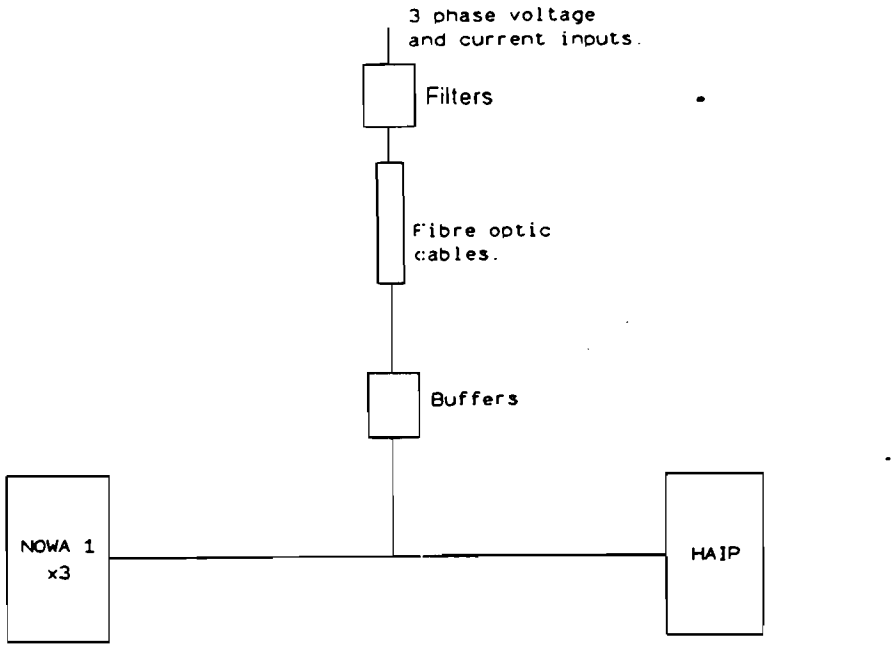
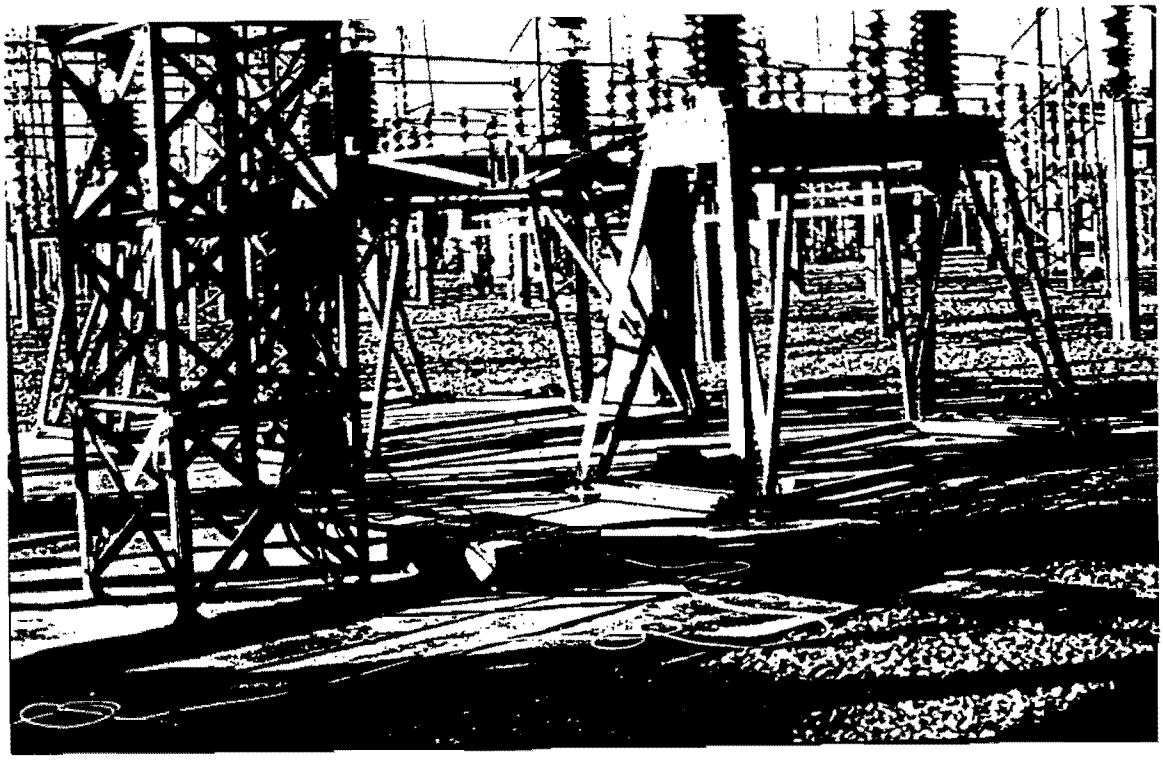


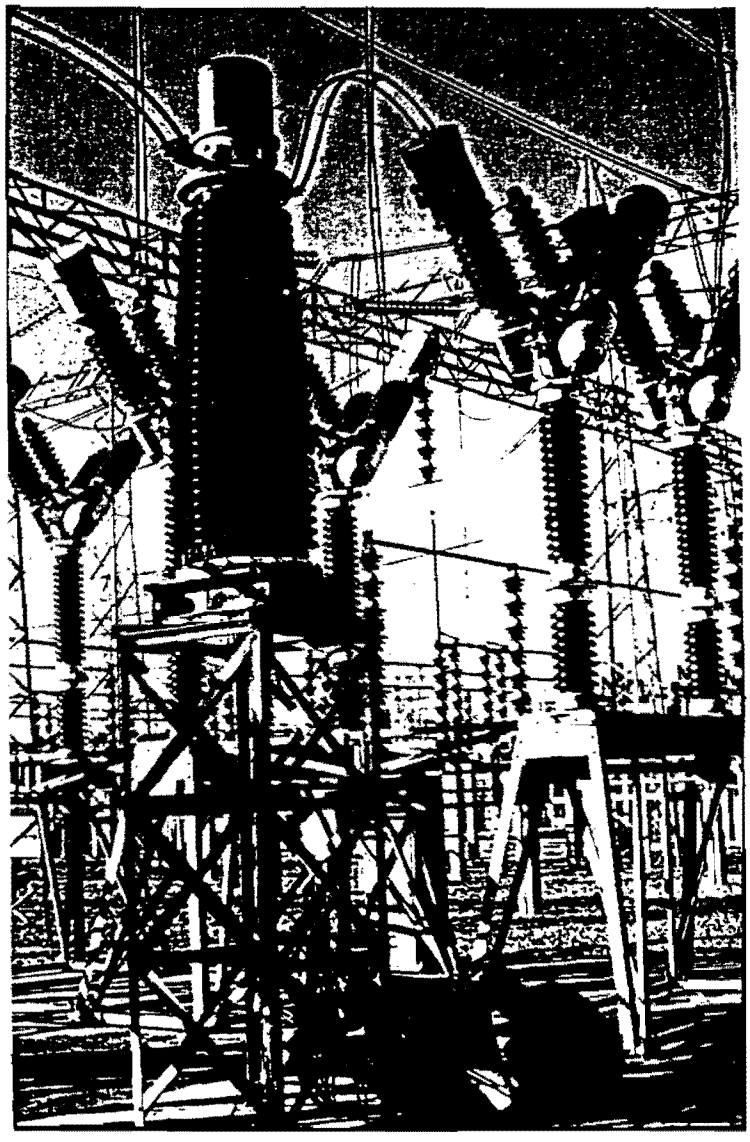
Figure 3: Connection of the harmonic monitors the Design Power's fibre optical measuring system.

the fundamental component in these signals, means that the harmonic monitor requires an external synchronising signal that follows the power system frequency. This was simply obtained from the 240V substation supply (which was also used as the power supply to the harmonic monitor). However, this is not possible at power stations where the station supply is provided by auxiliary generators (Benmore for instance). In this situation the output of a spare VT can be used to provide the external synchronising signal.

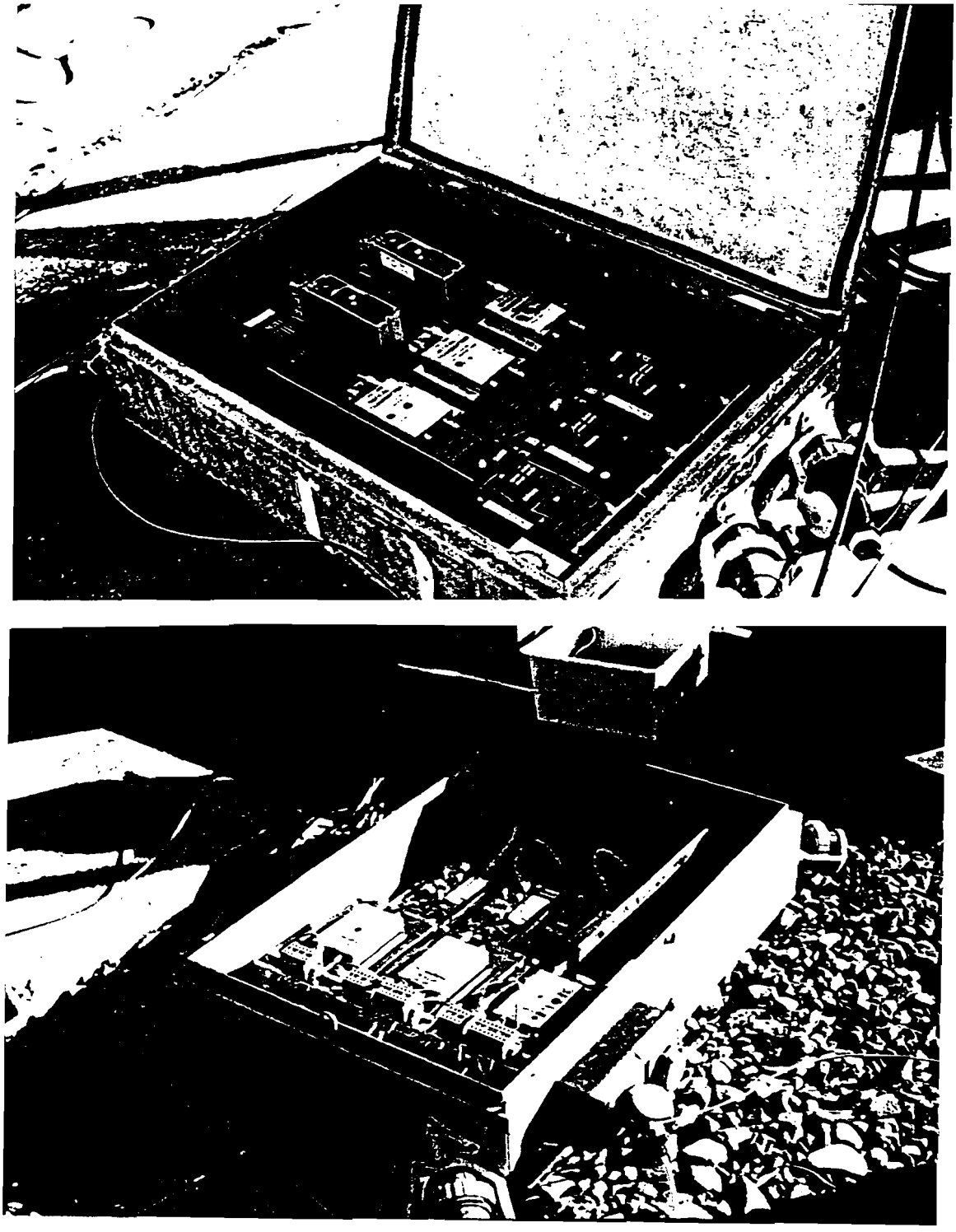
New Zealand substation power outlets use Reyrolle sockets, whereas the HAIP harmonic monitor power supply uses a standard New Zealand 3 pin plug. A Reyrolle plug to 3 pin socket converter is therefore required to enable harmonic monitoring.

The harmonic measurements performed were limited to 3 voltage channels and 2 current channels instead of the nominal 3 current channels. This was due to a fault in one channel of Design Power's current channel filters which was external to the HAIP harmonic monitor. The HAIP harmonic monitor was configured to acquire, analyse, monitor, and display the full six channels, although, because of the Design Power fault, was operated with one zero input channel. To demonstrate that this channel of the harmonic monitor was operational, the signal connected to channel 5 was briefly connected to channel 6, which performed correctly.



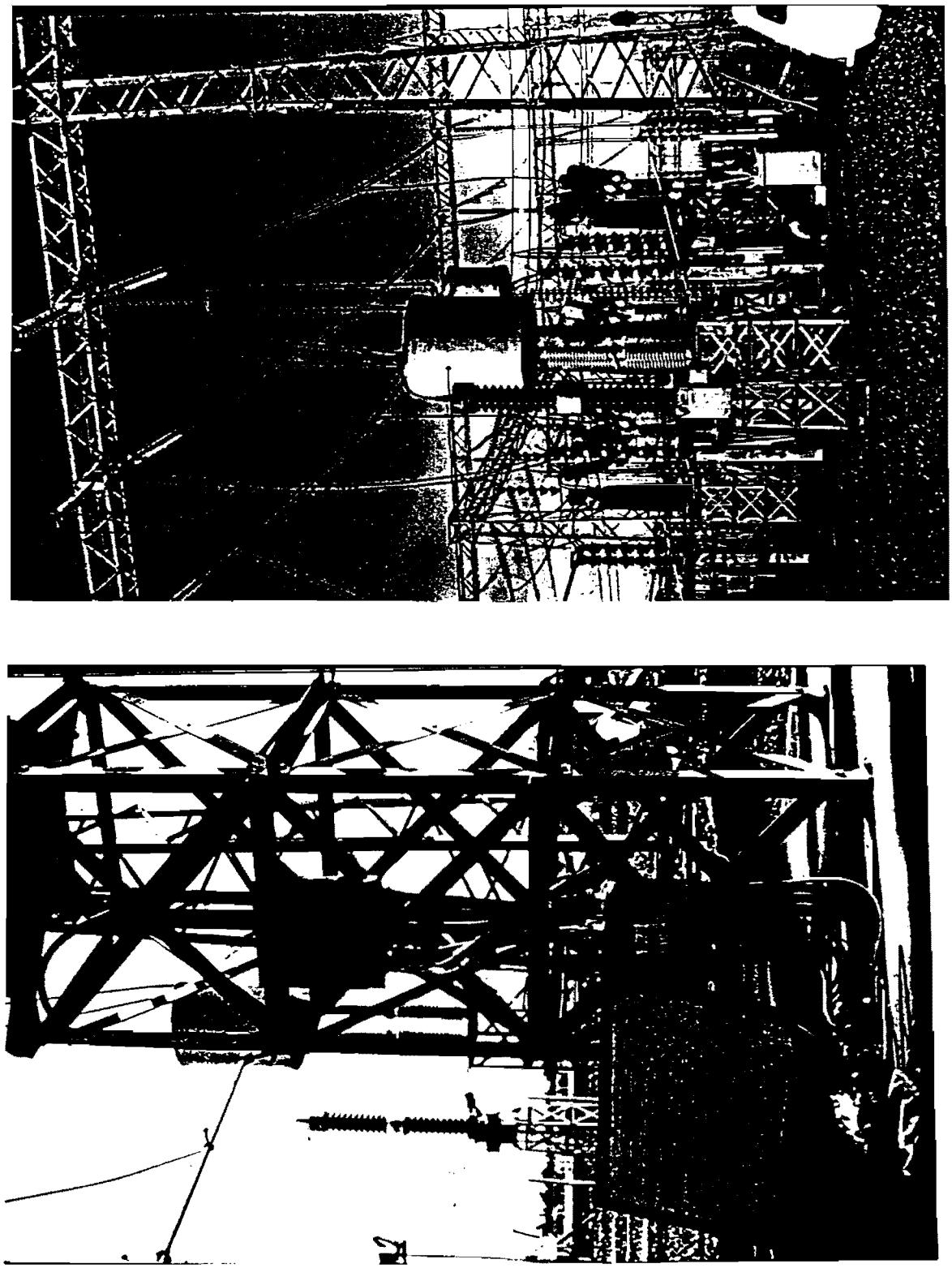


Above: The current channel filter cabinet located in the switch yard next to the CT post. *Right:* An Engineer inspects the current channel filter cabinet before closing it to begin monitoring.
Figure 4:



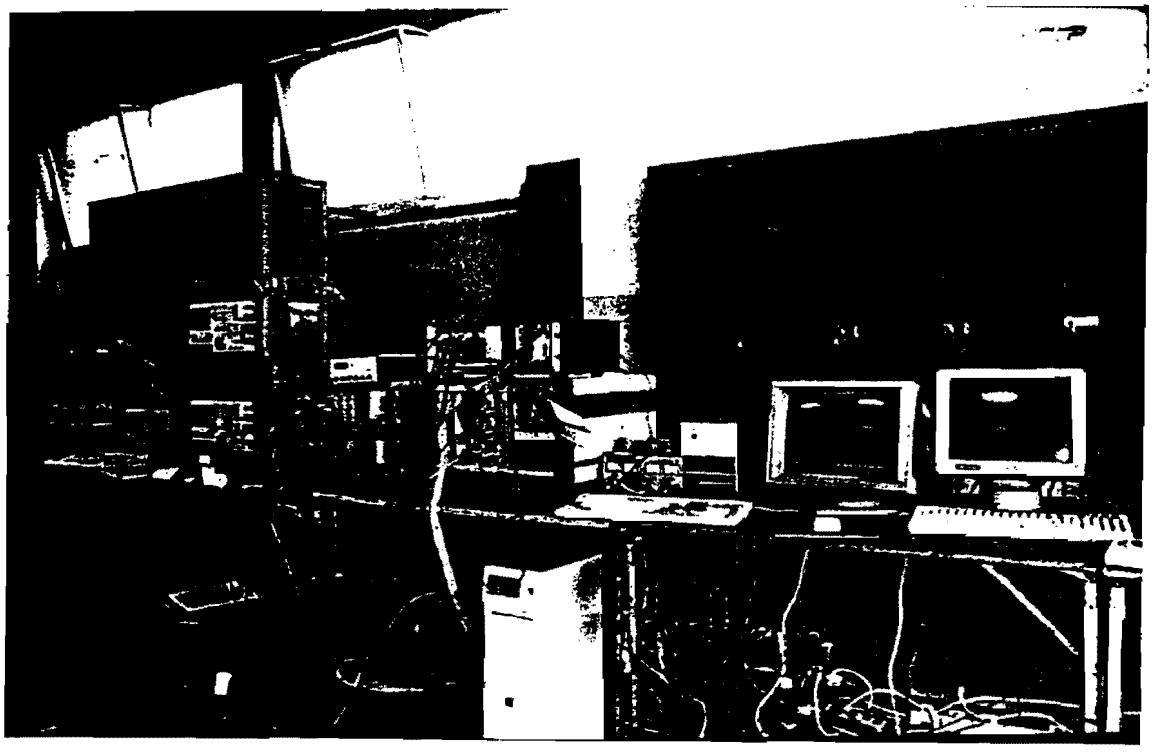
Above: The current channel filter cabinet. The cables connecting this to the spare CTs are situated on the right. Inside the cabinet are the current channel filters, the optical transmitters, and the power supplies for the active current channel filters. The precision resistors (Section 4.2.2) also inside the cabinet are not visible. The orange cables on the left are the fibre optical cables linking the harmonic monitoring instrumentation and filters. *Below:* The voltage channel filter cabinet. Inside the cabinet are the voltage channel filters and the optical transmitters. Power supplies for the passive voltage filters are not required. The fibre optical cable is visible in the foreground.

Figure 5:



Left: Current channel filter connections to the spare CTs on the CT post. *Right:* A Technician connects the voltage channel filter cabinet to the VT connections at the protection kiosk. A VT is visible in the foreground.

Figure 6:



The harmonic monitoring instrumentation. On the left is the Design Power equipment (3 NOWA-1s and a PC/AT), with the HAIP harmonic monitor in the centre right.

Figure 7:

3 THE FIBRE OPTICAL HARMONIC MEASURING SYSTEM

Design Power's fibre optical harmonic measuring system is used to safely interface harmonic monitoring instrumentation to VTs and CTs on an EHV power system. A typical harmonic measurement arrangement using this system is illustrated in Figure 8. The equipment is owned and operated by Design Power and consists of filters, optical transmitters, fibre optical cable, optical receivers, and buffers. It is an FM system, requiring an analog voltage input and providing an analog voltage output, and is specifically intended for analysis of signals on in-service high voltage equipment. The optical transmitters, receivers, and fibre optical cable were manufactured and supplied to Design Power by the Swiss company *Triskelion AG*. The filters and buffers are a Design Power addition, carried over from the New Zealand Electricity MAC-8 Harmonic Measuring System [13]. The filters are discussed in Section 3.2.

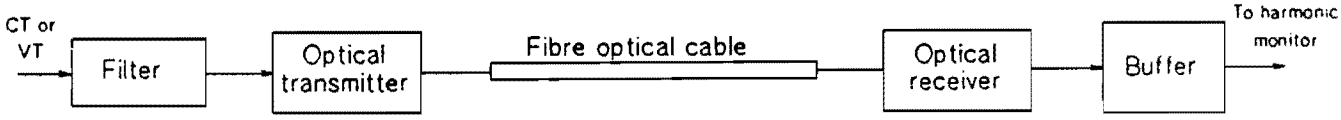


Figure 8: One channel of a typical harmonic measuring arrangement using the fibre optical harmonic measuring system.

3.1 Specifications

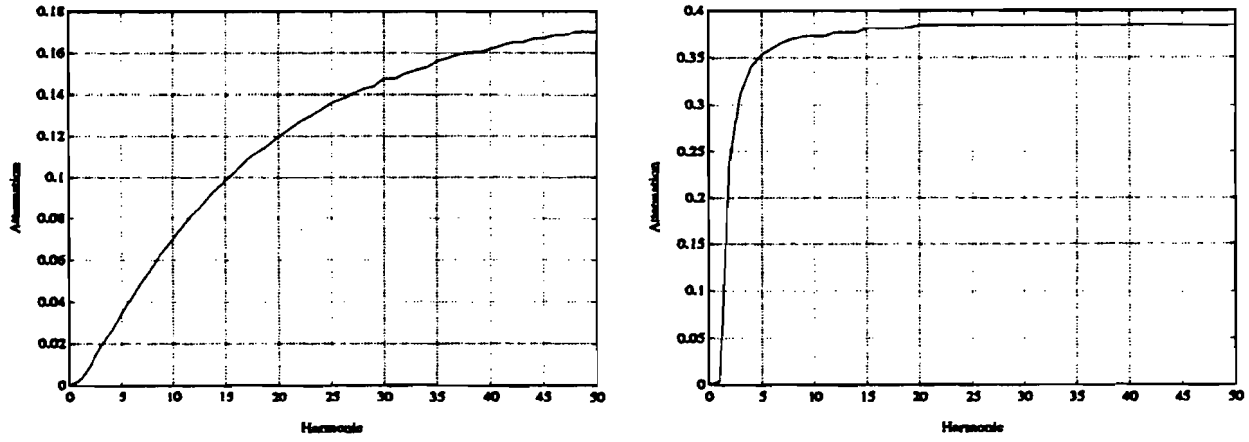
Limited information pertaining to the fibre optical transmission system has been supplied by Design Power. Included in this information are the specifications summarised below.

- Dynamic response 40 dB
- Signal to noise (max. signal) 46 dB
- Frequency range DC to 150 kHz (3 dB)

What is significant about these specifications is that the transmission system currently used to carry power system voltage and current signals from the measurement point to instrumentation for harmonic analysis has a dynamic range of 40 dB. To meet the legislative requirements [8], the voltage and current signals must be acquired with a dynamic range of at least 60 dB [1], [13], which means that the fibre optical transmission system's dynamic response is too low.

Design Power circumvent this problem by preceding their transmission system with high pass filters. The filters attenuate the fundamental frequency [13] to reduce the measured signals' dynamic ranges, enabling them to be transmitted by the fibre optical system without significant degradation caused by it's limited dynamic range. The filter magnitude response (combined with the optical transmission system and buffers) of the red phase channel is shown in Figure 9(a). The filters for the three voltage channels are identical in design. The Current channel filter and transmission system

magnitude response of the red phase is shown in Figure 9(b). These filters are also identical in design, but are different to the voltage channel filters. The reason for this difference can not be established.



(a) (b)

Figure 9: Red Phase Channel Filters: (a) Voltage, (b) Current.

3.2 Pre-filtering to Enhance Harmonics

The high pass filtering technique used by the Design Power system has been recommended [6] for use in systems with limited dynamic range, but requires compensation for the filters' responses if the harmonic results are to be related back to actual system parameters. This is achieved by multiplying the harmonics by the inverse filter responses, implemented in practice by multiplying harmonic results by lookup tables, determined from the filters in the laboratory. The phase response of the filters is compensated for by adding the inverse filter phase responses to the harmonic phase results. This compensation is a straightforward process requiring minimal computation and was used in this field test. The lookup tables used are listed in Appendix A.

These filter compensation lookup tables only contain compensation data for a fundamental frequency of 50.00Hz and harmonics of this. Because a power system is dynamic, it's fundamental frequency varies continuously around the nominal frequency of 50.00Hz. As the power system frequency varies, the harmonics move on the filter response curves of Figure 9. The filter response for low order harmonics is so steep that as they move on the response, their magnitude changes, introducing an error into the results from harmonic analysis, even after compensating for the filters using the method discussed previously. This effect is so pronounced that it was visible on the harmonic monitor's display during testing - as the power system frequency increased, the low order harmonics were seen to increase, and conversely, as it decreased, the low order harmonics were seen to decrease. The error introduced by this phenomenon is, however below that set in New Zealand legislation [8]. The derivation of equations giving the error in harmonic voltage and current is given in Appendix B, with the error in the first five voltage and current harmonics listed. Although the error in harmonic voltage and current is actually quite low, the error in the fundamental voltage is approximately 3% of the nominal phase-neutral system voltage, and the error in the fundamental current is approximately 60% of the line current.

If the fundamental magnitudes and phases are required it is necessary to use 'dynamic compensation' to reduce the error in them. This can be implemented in two ways. Filters with inverse magnitude and phase responses to the voltage and current channel filters can be inserted into the analog signal path preceding the harmonic monitor, thereby dynamically compensating for the fundamental and all

harmonics. Alternatively, the fundamental components can be dynamically compensated in software after harmonic analysis by fitting interpolating functions to the voltage and current channel filter responses about the fundamental. These functions are dependent on system frequency and must be evaluated each time the fundamental is to be compensated.

The fundamental components are required to find individual harmonic percentages (Equation 1), total harmonic distortion (Equation 2), equivalent disturbing voltage (Equation 3), and equivalent disturbing current (Equation 4) [5], [6].

$$C_n^* = 100\frac{c_n}{c_1}\ \%. \tag{1}$$

$$THD = 100\frac{\sqrt{\left(\sum_{n=2}^{\infty} c_n^2\right)}}{c_1}\ \%. \tag{2}$$

$$EDV = \frac{1}{P_{800}}\sqrt{\sum_{n=1}^{50}(nP_nU_n)^2} \tag{3}$$

$$EDI = \frac{1}{P_{800}}\sqrt{\sum_{n=1}^{50}(nP_nI_n)^2} \tag{4}$$

New Zealand legislation, however, relates these quantities to the nominal system voltage (for voltage harmonics), or simply uses absolute Amps. (for current harmonics) and therefore does not require the fundamental components. For example, the fundamental component (c_1) in Equations 1 and 2 is replaced by the nominal system voltage and the summations in Equations 3 and 4 are between the second harmonic ($n = 2$) and the 50^{th}.

4 THE RELATION OF OBSERVED RESULTS TO ACTUAL POWER SYSTEM VOLTAGE AND CURRENT

4.1 Data Acquisition System Input

The HAIP harmonic monitor processing is arranged so that a sine wave input of the maximum allowable amplitude (±10 Volts peak) produces a full scale output (the first harmonic is the only visible harmonic and reaches full scale which is 10 divisions).

For the general case where a particular harmonic indicates n divisions on the display, with $0 \leq n \leq 10$, the contribution of that particular harmonic to the input voltage is given by the equation

$$Vin = \frac{n}{10} Vpeak, \tag{5}$$

where

$$Vpeak = 10Volts. \tag{6}$$

Substituting Equation 6 into Equation 5 yields

$$Vin = n. \tag{7}$$

If the front end of the data acquisition system has a gain of g, then

$$Vin = \frac{n}{g}, \tag{8}$$

and the rms contribution of a particular harmonic to the signal acquired by the data acquisition system is given by

$$Vin(rms) = \frac{n}{\sqrt{2}g} \; Volts. \tag{9}$$

The signals from the VTs and CTs are passed through filters which severly attenuate the low order harmonics - particularly the fundamental frequency. This distortion is compensated for in the frequency domain by multiplying the harmonic results by the filters' inverse transfer functions (in the form of compensation tables) as illustrated in Figure 10. The filtering and compensation are discussed in greater detail in Section 3. The compensation tables were calculated from the filter responses determined in the Electrical and Electronic Engineering Department laboratory before the tests, and are listed in Appendix A. The results displayed (n) can therefore be related directly to the measured signal, Vin (derived from the VTs and CTs). The filter compensation tables incorporate the filters, the fibre optical transmission system, and the buffers shown in Figure 3. Because the filters in Design Power's fibre optical measuring system are compensated for, Equation 9 is still valid, and the displayed results can be related directly to the filter input voltages. Filter compensation is discussed in more detail in Section 3.2.

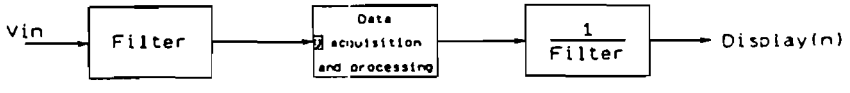


Figure 10: Filter compensation

4.2 Relating Displayed Results to System Voltage and Current

4.2.1 Determination of Line Voltage

The VTs are connected between phase and neutral of each phase as depicted in Figure 11, giving a secondary voltage

$$V_s = \frac{V_p}{a}, \tag{10}$$

where V_p is the primary VT voltage or line phase to neutral voltage and a is the VT ratio.

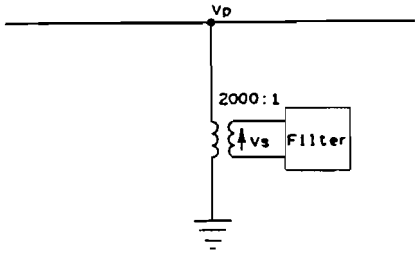


Figure 11: VT connection

Since the filter input voltage is known (Equation 9, Section 4.1) it is possible to find the system phase voltage.

Substituting $Vin(rms)$ of Equation 9 for V_s in Equation 10 gives

$$\frac{n}{\sqrt{2}g} = \frac{V_p}{a}. \tag{11}$$

Rearranging this equation gives

$$V_p(rms) = \frac{na}{\sqrt{2}g}\ Volts. \tag{12}$$

Given the VT ratio and the data acquisition system gain, the harmonic voltage corresponding to a displayed harmonic can be determined using Equation 12.

4.2.2 Determination of Line Current

The current transformers give a secondary current

$$I_s = \frac{I_p}{a}, \tag{13}$$

where I_p is the primary CT current or line current and a is the CT ratio, illustrated in Figure 12.

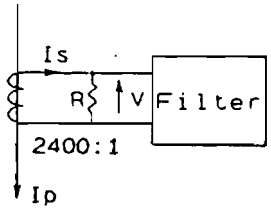


Figure 12: CT connection

This secondary current is passed through a precision wire wound resistor, producing a voltage

$$V = I_s R, \tag{14}$$

where R is the resistor's resistance in Ohms. Substituting Equation 13 into Equation 14 gives

$$V = \frac{I_p R}{a}. \tag{15}$$

The filter input voltage is given by Equation 9 (Section 4.1). Substituting $Vin(rms)$ of Equation 9 for V in Equation 15 gives

$$\frac{n}{\sqrt{2}g} = \frac{I_p R}{a}. \tag{16}$$

Rearranging this equation yields

$$I_p(rms) = \frac{an}{\sqrt{2}gR}\ Amps \tag{17}$$

Given the CT ratio, the value of R, and the data acquisition system gain, the harmonic current corresponding to a displayed harmonic can be determined using Equation 17.

5 PRELIMINARY RESULTS

5.1 Harmonic Results

Harmonic results from the harmonic monitor compared favourably with the Design Power NOWA-1 harmonic monitors' results. Harmonic data was stored at various times during the test with the intention of using it to test improvements to the display system, discussed in Section 6. Photographs of the harmonic monitor display taken while monitoring are shown in Figure 13. The photographs were taken on July 26, with the station loadings recorded at approximately the same time. These are shown in Figure 14.

The gains of the data acquisition system voltage channels were manually set and maintained at $\times 10$ throughout the tests, while the gains of the current channels were set at $\times 50$. The fibre optical transmission system current channels were set up with a gain of $\times 5$, giving a total current channel gain of $\times 250$.

Dropping n from Equation 12 of Section 4.2.1 gives the voltage channel scale

$$V_p(rms) = \frac{a}{\sqrt{2}g}\ Volts/division, \tag{18}$$

where

$a = 2000$ - the ratio of the VT used in the test,

and

$g = 10$.

Therefore $V_p(rms) \simeq 141 Volts/division$.

Similarly for current, dropping n from Equation 17 of Section 4.2.2 gives the current channel scale

$$I_p(rms) = \frac{a}{\sqrt{2}gR}\ Amperes/division, \tag{19}$$

where

$a = 2400$ - the ratio of the CT used in the test,

$R = 15\Omega$ - the precision wire wound resistor value,

and

$g = 250$.

Therefore $I_p(rms) \simeq 0.453 Amperes/division$.

The fundamental components in Figure 13 are compressed because they were not multiplied by their compensation values. This allows close inspection of harmonics, and as shown in Appendix B, the error in measuring fundamental voltage and current is large (because of the very steep magnitude response of the Design Power filters discussed in Section 3). The yellow phase current is not apparent in Figure 13. This is due to the fault on one current channel of the Design Power harmonic measuring system, as mentioned in Section 2.

5.2 Noise Tests

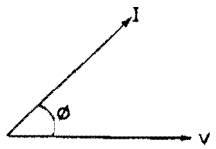
To ascertain the noise levels present at the output of the Design Power harmonic measuring system, all of the current and voltage channels were short circuited in the switch yard and the output of the system was monitored with an oscilloscope. With the HAIP harmonic monitor disconnected, the noise level was negligible, however, when it was connected a signal of approximately 25MHz was observed. This signal was 60dB below the maximum signal level on all current channels and 50 dB below the maximum signal level on all voltage channels. A possible cause of this is improper grounding of the harmonic monitoring instrumentation. The level of this noise was seen to increase when a TAIT Electronics hand held radio was used to communicate from the relay room (the site of the instrumentation) to the switch yard.

5.3 Notable features of the NOWA-1s

The opportunity during the field test to operate the Design Power NOWA-1 harmonic monitors was used to record their more notable features. These are listed below.

- A cursor is provided to enable a user to select a particular harmonic and read it's magnitude.

- Phase angle between harmonic voltage and current (shown below) can be displayed - as power factor ($cos\phi$).



- A logarithmic harmonic magnitude display option is provided.

- It has a hard copy facility.

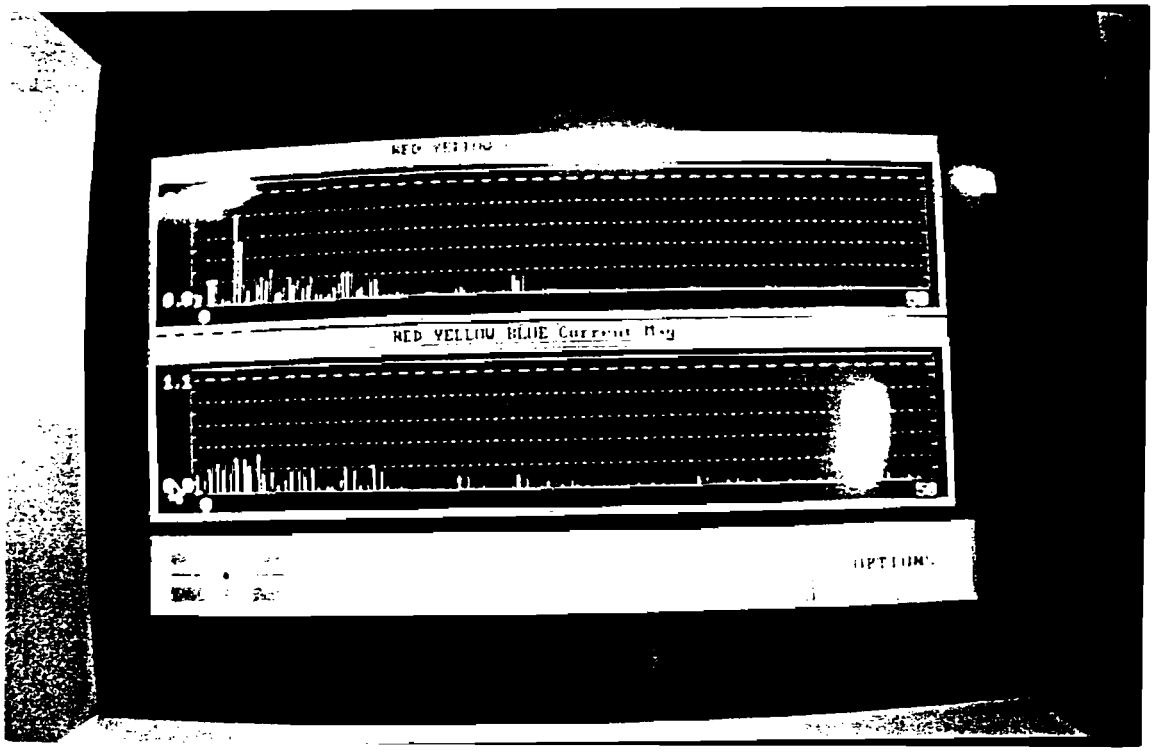
- It's graduated display gives meaningful harmonic levels (in Volts and Amps.) when its own CTs and VTs are used.

- It can display an expanded spectrum from the fundamental to the 25^{th} harmonic.

- It can display up to the 50^{th} harmonic.

- It can show the spectrum one harmonic either side of a selected harmonic.

- The sampled time domain input signal can be displayed.



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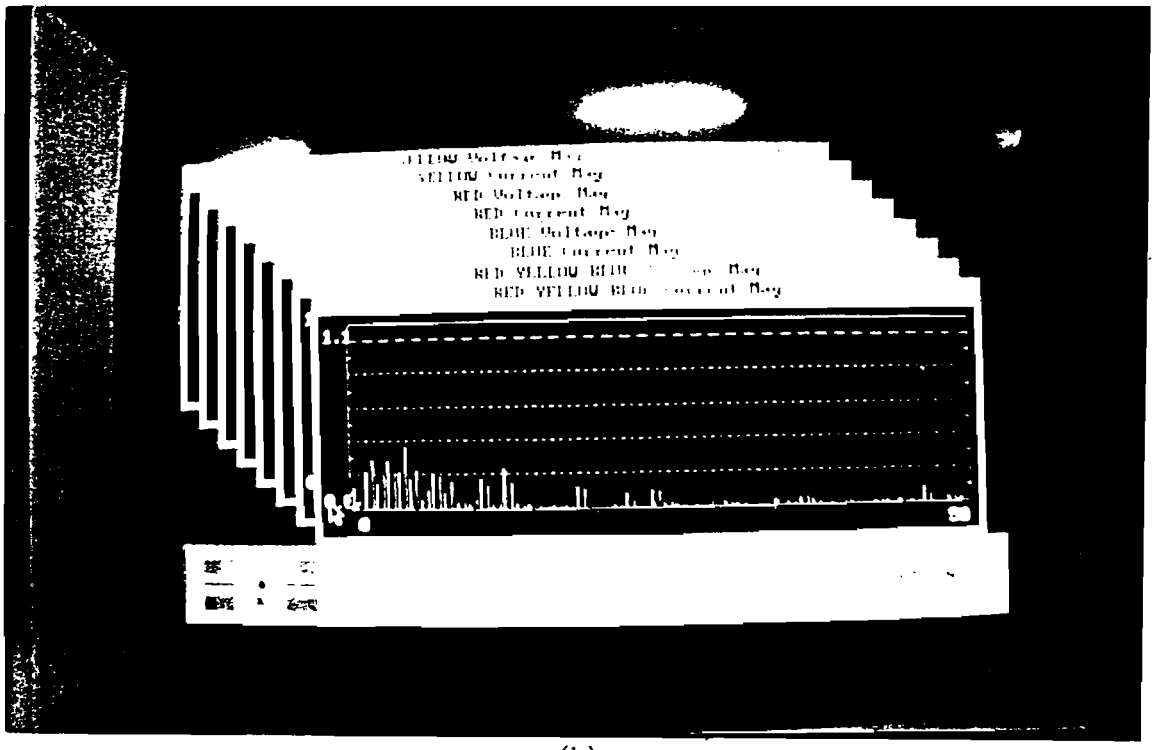
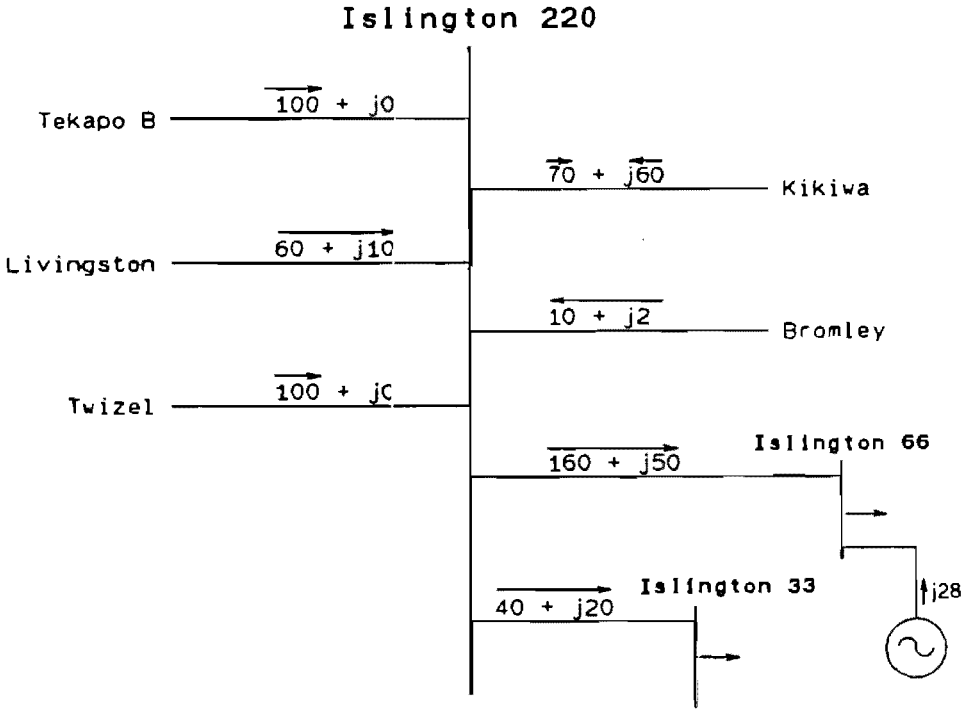


(b)

Figure 13:
Harmonic monitor displays. The voltage scale is 141 Volts/division, and the current scale is 0.453 Amps./division. (a) Voltage and current harmonics measured at 1:27 pm on July 26, 1990. The fundamental frequency is 49.95Hz. (b) Current harmonics measured at 2:34 pm on July 26, 1990. The fundamental frequency is 50.10Hz.



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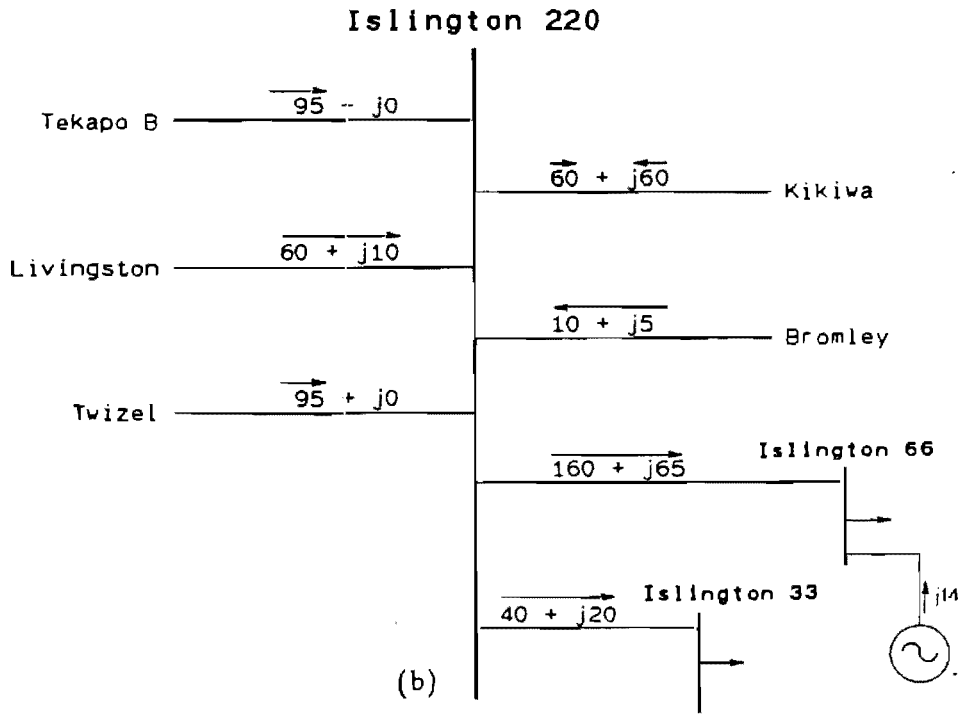

(b)

Figure 14: Station loadings. (a) 1:13 pm on July 26, 1990. (b) 2pm on July 26, 1990.

6 FUTURE DEVELOPMENT

Continuing development of harmonic monitoring instrumentation within the power systems research group will come under the title "CHART" (Continuous Harmonic Analysis in Real Time) and will involve improvements to the following areas:

- Data acquisition system.
- Processing capability.
- On-line analysis of harmonics.
- User interface and harmonic display.

The improved data acquisition system will incorporate a calibration source, enabling the instrument to automatically determine compensation tables for front end filters and other signal conditioning equipment.

The increased processing capability [3] (gained through upgrading the computer system) will enable DFTs (discrete Fourier transforms) to be computed over more than one cycle, enabling an expanded spectrum about an harmonic to be displayed. It will also enable more complex on-line analysis algorithms to operate on harmonic data, reducing the instruments storage requirements and the amount of post-processing of harmonic data required. The increased processing capability will also enable every computer in the instrument to run an operating system. This will decrease software development time and allow more flexibility when designing and upgrading software.

The upgraded computer system contains a graphical interface which has a terminal emulation facility - it emulates a terminal for each computer in the system using a window environment. This makes the instrument more portable, as only one terminal is required to operate the computers, whereas with the present system, one terminal is required for each computer.

The user interface will be improved by using the signal analysis package ASYST (A Scientific System) running on a PC/AT. This has a menu feature, allowing simple configuration and operation of the instrument. The user will be able to configure the instrument for a particular system by entering the nominal system voltage, CT and VT ratios, and what compensation data (if any) for the CTs, VTs, and harmonic measuring interface is required. All of these parameters will be available from a data base of standard CTs and VTs.

Harmonic displays will include line voltage and current harmonics, power factor, active and reactive power harmonics, and impedance loci. These will be displayed on either logarithmic or linear axes, with automatic scale calculation and display, relating the displays to actual power system units. A hard copy generation facility will also be provided.

The use of ASYST introduces tremendous flexibility into the instrument interface design, enabling the simple addition of further display options when required.

7 CONCLUSION

The field test showed that the harmonic monitor can be moved from the laboratory to the field and used to make harmonic measurements of a power system when interfaced to the power system using the Design Power harmonic measuring system. The test highlighted features that the monitor must have for it to be a useful in the analysis of power system harmonics and pointed towards an upgraded configuration for the harmonic monitor. These features include: the calculation of power and impedance; automatic scale calculation relating displayed results to actual parameters; improved on-line analysis; the use of standard software for the user interface; and improved portability.

The overall accuracy of the harmonic monitor's results is dependent upon the ability of Electricorp's current and voltage transducers and interface system to provide accurate replicas of the power system waveforms. The harmonic monitor can guarantee accurate analysis given these accurate replicas.

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A FILTER COMPENSATION TABLES

This appendix lists the tables of compensation data for Design Power harmonic measuring system. The tables were computed from the systems response, determined in the Electrical and Electronic Engineering laboratory in July 1990. Each table is arranged as a group of 51 magnitude compensation values, followed by a group of 51 phase compensation values, for the three voltage phases and the three current phases. The first number (on a separate row) in each group corresponds to the dc result from the FFT, with the remaining numbers corresponding to harmonics (the first harmonic (fundamental) is on the top left, while the 50^{th} harmonic is on the bottom right).

Table 1 lists the compensation parameters actually used by the HAIP harmonic monitor in the July 1990 field test. Notice that the fundamental compensation value is 1. This maintains it at a low level, allowing closer inspection of the harmonics. The phase compensation tables are all zero - phase shift was not compensated for in the test, although the phase of any stored harmonic data can be compensated for during further analysis.

Table 2 lists the actual compensation data for the fibre optical measuring system. Harmonic magnitudes are compensated for by multiplying by the magnitude values tabulated, while harmonic phase is compensated for by adding the phase values tabulated.

INTERFACE.CMP - table 1

/* Channel one (red phase voltage) */

1.									
1.	106.18	53.47	38.12	28.94	23.71	20.06	17.59	15.59	14.24
13.06	12.12	11.35	10.65	10.12	9.71	9.24	8.94	8.65	8.35
8.12	7.88	7.71	7.53	7.35	7.24	7.12	7.	6.94	6.76
6.76	6.65	6.59	6.53	6.41	6.35	6.29	6.24	6.24	6.18
6.12	6.06	6.06	6.	6.	5.94	5.94	5.88	5.88	5.88
0.									
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.

/* Channel two (yellow phase voltage) */

1.									
1.	108.18	56.82	38.59	29.35	23.94	20.29	17.76	15.76	14.35
13.18	12.24	11.47	10.76	10.24	9.59	8.76	9.	8.71	8.41
8.18	8.	7.76	7.59	7.41	7.29	7.18	7.06	6.94	6.84
6.76	6.71	6.59	6.53	6.47	6.41	6.35	6.29	6.24	6.18
8.18	6.12	6.06	6.06	6.	6.	5.94	5.94	5.88	5.88
0.									
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.

/* Channel three (blue phase voltage) */
1.
1. 106.41 54.76 38.12 28.82 23.76 20.06 17.59 15.65 14.24
13.12 12.18 11.41 10.71 10.14 9.74 9.27 8.95 8.68 8.37
8.14 7.94 7.74 7.58 7.41 7.29 7.17 7.05 6.95 6.82
6.77 6.67 6.6 6.53 6.4 6.33 6.33 6.27 6.26 6.2
6.15 6.11 6.08 6.08 6.04 6.01 5.95 5.92 5.9 5.88

0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.

/* Channel four (red phase current) */
1.
1. 4.16 3.22 2.94 2.83 2.78 2.73 2.7 2.68 2.68
2.68 2.65 2.65 2.65 2.62 2.62 2.62 2.62 2.62 2.6
2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6
2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6
2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6

0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.

/* Channel five (yellow phase current) */
1.
1. 4.29 3.27 2.96 2.86 2.78 2.75 2.73 2.7 2.7
2.68 2.68 2.68 2.65 2.62 2.65 2.62 2.62 2.62 2.6
2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6
2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6
2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6 2.6

0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.
0. 0. 0. 0. 0. 0. 0. 0. 0. 0.

/* Channel six (blue phase current) */

1.

1.	4.29	3.3	2.99	2.88	2.83	2.78	2.75	2.73	2.73
2.7	2.7	2.7	2.68	2.65	2.68	2.65	2.65	2.65	2.62
2.65	2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62
2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62
2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62

0.

0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
0.	0.	0.	0.	0.	0.	0.	0.	0.	0.

ACTUAL.CMP - table 2

/* Channel one (red phase voltage) */

1.

376.29	106.18	53.47	38.12	28.94	23.71	20.06	17.59	15.59	14.24
13.06	12.12	11.35	10.65	10.12	9.71	9.24	8.94	8.65	8.35
8.12	7.88	7.71	7.53	7.35	7.24	7.12	7.	6.94	6.76
6.76	6.65	6.59	6.53	6.41	6.35	6.29	6.24	6.24	6.18
6.12	6.06	6.06	6.	6.	5.94	5.94	5.88	5.88	5.88

0.

-190.	-160.5	-137.1	-123.6	-114.8	-106.1	-100.2	-94.9	-90.6	-86.2
-82.9	-79.5	-76.5	-73.5	-71.	-69.1	-66.7	-64.6	-62.5	-61.
-59.1	-57.3	-55.9	-54.5	-53.1	-51.8	-50.4	-49.1	-48.	-47.1
-45.9	-44.9	-44.	-42.9	-41.9	-41.4	-40.8	-40.	-39.2	-38.3
-37.7	-37.1	-36.6	-35.9	-35.2	-34.7	-34.3	-33.7	-33.4	-33.

/* Channel two (yellow phase voltage) */

1.

593.71	108.18	56.82	38.59	29.35	23.94	20.29	17.76	15.76	14.35
13.18	12.24	11.47	10.76	10.24	9.59	8.76	9.	8.71	8.41
8.18	8.	7.76	7.59	7.41	7.29	7.18	7.06	6.94	6.84
6.76	6.71	6.59	6.53	6.47	6.41	6.35	6.29	6.24	6.18
8.18	6.12	6.06	6.06	6.	6.	5.94	5.94	5.88	5.88

0.

-190.	-160.6	-138.1	-124.	-114.3	-106.5	-100.6	-95.2	-91.1	-86.7
-88.4	-79.9	-77.	-74.1	-71.5	-69.7	-67.4	-65.2	-63.2	-61.8
-59.4	-58.2	-57.7	-55.4	-54.	-52.8	-53.3	-50.	-49.	-47.9
-47.	-45.9	-45.2	-44.	-43.	-42.5	-41.5	-41.3	-40.4	-39.5
-39.	-38.4	-37.9	-37.2	-36.5	-36.1	-35.9	-35.2	-34.8	-34.6

/* Channel three (blue phase voltage) */

1.

497.82	106.41	54.76	38.12	28.82	23.76	20.06	17.59	15.65	14.24
13.12	12.18	11.41	10.71	10.14	9.74	9.27	8.95	8.68	8.37
8.14	7.94	7.74	7.58	7.41	7.29	7.17	7.05	6.95	6.82
6.77	6.67	6.6	6.53	6.4	6.33	6.33	6.27	6.26	6.2
6.15	6.11	6.08	6.08	6.04	6.01	5.95	5.92	5.9	5.88

0.

-190.	-159.6	-138.9	-124.1	-114.1	-106.1	-100.2	-94.8	-90.4	-86.2
-82.8	-79.4	-76.5	-73.4	-71.	-69.1	-66.8	-64.6	-62.4	-61.1
-59.1	-57.5	-55.5	-54.5	-53.	-51.8	-50.5	-49.1	-48.1	-47.2
-46.1	-45.	-44.2	-43.1	-41.5	-40.8	-40.8	-40.2	-39.3	-38.5
-38.	-37.4	-36.2	-36.	-35.6	-35.	-34.5	-33.4	-33.6	-33.2

/* Channel four (red phase current) */

1.

237.71	4.16	3.22	2.94	2.83	2.78	2.73	2.7	2.68	2.68
2.68	2.65	2.65	2.65	2.62	2.62	2.62	2.62	2.62	2.6
2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6
2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6
2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6

0.

-90.	-51.8	-35.1	-26.8	-22.5	-18.8	-16.5	-14.9	-13.2	-12.3
-11.8	-10.9	-10.5	-9.6	-9.3	-9.5	-9.3	-8.9	-8.6	-8.8
-8.5	-8.2	-8.3	-8.2	-8.1	-8.0	-7.7	-7.8	-7.8	-7.7
-7.7	-7.7	-7.7	-7.7	-7.7	-7.7	-7.7	-7.7	-7.7	-7.7
-7.7	-7.7	-7.7	-7.7	-7.7	-7.7	-7.7	-7.7	-7.7	-7.7

/* Channel five (yellow phase current) */

1.

207.66	4.29	3.27	2.96	2.86	2.78	2.75	2.73	2.7	2.7
2.68	2.68	2.68	2.65	2.62	2.65	2.62	2.62	2.62	2.6
2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6
2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6
2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6	2.6

0.

-90.	-52.9	-36.2	-27.8	-23.3	-19.4	-17.	-15.3	-14.1	-12.7
-12.2	-11.2	-10.7	-9.9	-9.5	-9.6	-9.4	-9.0	-8.5	-8.8
-8.5	-8.2	-8.3	-8.2	-8.1	-8.0	-7.8	-7.6	-7.6	-7.6
-7.6	-7.6	-7.6	-7.6	-7.6	-7.6	-7.6	-7.6	-7.6	-7.6
-7.6	-7.6	-7.6	-7.6	-7.6	-7.6	-7.6	-7.6	-7.6	-7.6

/* Channel six (blue phase current) */

1.

171.4	4.29	3.3	2.99	2.88	2.83	2.78	2.75	2.73	2.73
2.7	2.7	2.7	2.68	2.65	2.68	2.65	2.65	2.65	2.62
2.65	2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62
2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62
2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62	2.62

0.

-90.	-52.1	-35.8	-27.4	-22.9	-19.1	-16.7	-15.	-14.	-12.5
-11.8	-11.	-10.4	-9.7	-9.3	-9 4	-9.1	-8.7	-8.3	-8.2
-7.9	-8.	-7.4	-7.8	-7.5	-7 3	-7.3	-7.3	-7.2	-7.2
-7.2	-7.2	-7.2	-7.2	-7.2	-7 2	-7.2	-7.2	-7.2	-7.2
-7.2	-7.2	-7.2	-7.2	-7.2	-7 2	-7.2	-7.2	-7.2	-7.2

B ERROR INTRODUCED BY FILTERING

This appendix develops approximate relationships for the error, introduced by the Design Power harmonic measuring system, in measuring harmonic voltage and current caused by fundamental frequency variations.

Equation 12 of Section 4.2.1 gives the harmonic voltage corresponding to a displayed harmonic. Rearranging this equation for the number of divisions displayed on the harmonic monitors display for a particular harmonic voltage on the power system yields

$$n = \frac{\sqrt{2}V_p g}{a} \ divisions. \tag{20}$$

The voltage channel filter of Figure 10, with response shown in Figures 9(a) and 15(a), will attenuate the harmonic voltage V_p by $A(f)$ where $A(f)$ is a function of power system frequency, f. This yields the attenuated harmonic voltage

$$V_p' = A(f)V_p. \tag{21}$$

Substituting this into Equation 20 yields

$$n' = \frac{\sqrt{2}A(f)V_p g}{a}. \tag{22}$$

The filter attenuation is compensated for by multiplying by the lookup table value C, which is constant for a particular harmonic, regardless of frequency. Multiplying Equation 22 by C yields the compensated value displayed by the harmonic monitor,

$$n'' = \frac{\sqrt{2}A(f)V_p g}{a}C. \tag{23}$$

New Zealand legislation [8] states that harmonic measurements shall be made when the system frequency is within 0.5 percent above or below the standard of 50Hz. This provides limits for Equation 23. If the fundamental frequency is represented by f_0, and f_1 and f_2 represent frequencies 0.5 percent above and 0.5 percent below an harmonic frequency, f_1 and f_2 are given by:

$$f_1 = (1.005)hf_0,$$

and

$$f_2 = (0.995)hf_0.$$

where h is the harmonic order.

Substituting f_1 and f_2 into Equation 23 gives

$$n''_{f1} = \frac{\sqrt{2}A(f_1)V_p g}{a}C, \tag{24}$$

and

$$n''_{f2} = \frac{\sqrt{2}A(f_2)V_p g}{a}C. \tag{25}$$

Substituting these into Equation 12 of Section 4.2.1 gives the measured harmonic voltages

$$V_{pf1} = A(f_1)CV_p, \tag{26}$$

and

$$V_{pf2} = A(f_2)CV_p, \tag{27}$$

where V_p is the actual harmonic voltage.

The error in measured voltage caused by the fundamental frequency changing between it's limits is given by

$$\Delta V = |V_{pf1} - V_{pf2}|. \tag{28}$$

Substituting V_{pf1} and V_{pf2} into this equation yields

$$\Delta V = V_pC|A(f_1) - A(f_2)|. \tag{29}$$

If the filter magnitude response at an harmonic is approximated by the linear equation

$$A(f) \simeq a_1 f + b_1, \tag{30}$$

Equation 29 reduces to

$$\Delta V \simeq V_pCa_1\Delta f, \tag{31}$$

where

$$\Delta f = \frac{1}{2}h. \tag{32}$$

Substituting this into Equation 31 yields

$$\Delta V \simeq \frac{1}{2}V_pCha_1. \tag{33}$$

The approximate error in measuring an harmonic voltage due to fundamental frequency fluctuations is given by one half of the product of the actual harmonic voltage (V_p), the slope (a_1) of the highpass filter response (Figure 15(a)) at the harmonic, and the harmonic order (h).

Similarly for current,

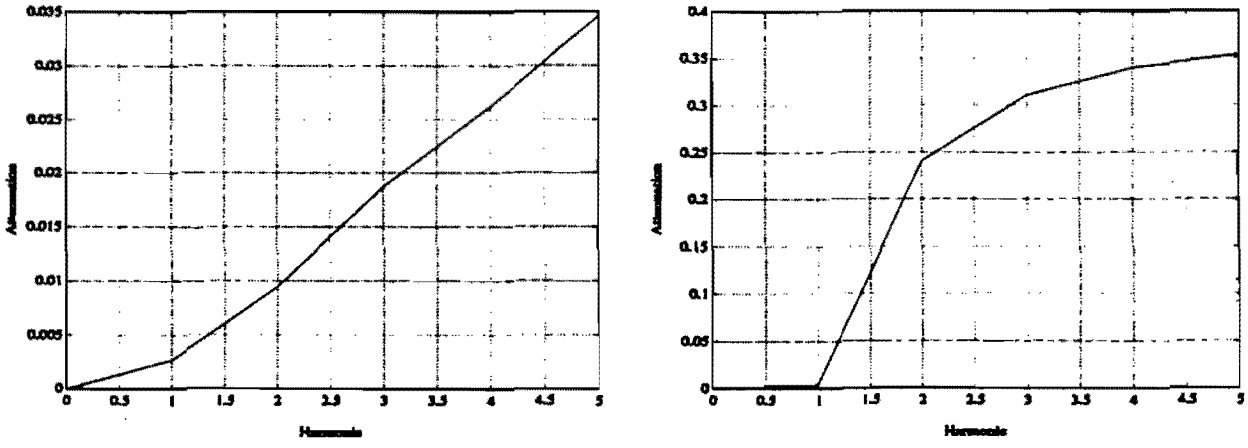
$$\Delta I \simeq \frac{1}{2}I_pCha_1. \tag{34}$$

The approximate error in measuring an harmonic current due to fundamental frequency fluctuations is given by one half of the product of the actual harmonic current (I_p), the slope (a_1) of the highpass filter response (Figure 15(b)) at the harmonic, and the harmonic order (h).

The error in measuring the harmonic voltage for the first five harmonics is shown in Table 1. The maximum allowable harmonic voltages were obtained from New Zealand legislation [8] with a nominal system voltage of 220KV. A representative fundamental voltage was taken as 100% of the nominal phase-neutral system voltage.

The error in measuring the harmonic current for the first five harmonics is shown in Table 2. The maximum allowable harmonic currents were obtained from New Zealand legislation [8]. A representative fundamental current was taken as 100% of the actual line current.

Figure 16 shows the phase responses of the fibre optical transmission system and high-pass filters.



(a) (b)

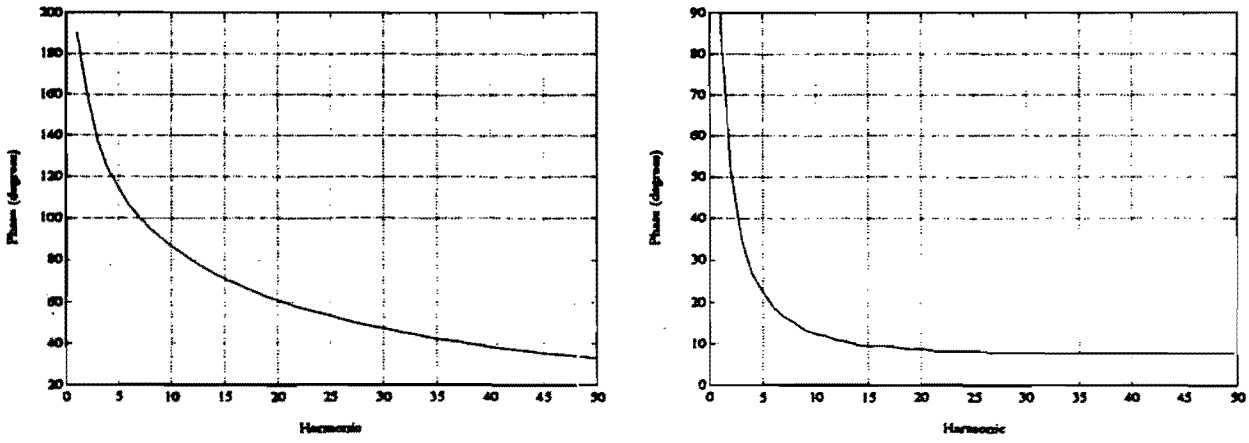
Figure 15: Red Phase Channel Filters - magnitude response: (a) Voltage, (b) Current.

Harmonic order (h).	Approximate filter slope at h (a_1, Hz^{-1}).	Maximum allowable harmonic voltage (V_p) expressed as a percentage of the nominal phase-neutral system voltage.	Filter compensation value (C).	Approximate error (ΔV) in measured harmonic voltage expressed as a percentage of the nominal phase-neutral system voltage.
1	1.6×10^{-4}	100%	376.29	3%
2	1.6×10^{-4}	1.2%	106.18	0.02%
3	1.6×10^{-4}	2.3%	53.47	0.03%
4	1.6×10^{-4}	0.6%	32.12	0.006%
5	1.6×10^{-4}	1.4%	28.94	0.02%

Table 1: Error in measured harmonic voltage.

Harmonic order (h).	Approximate filter slope at h (a_1, Hz^{-1}).	Maximum allowable harmonic current (I_p) (Amperes). The fundamental is given as a percentage of line current.	Filter compensation value (C).	Approximate error (ΔI) in measured harmonic current (Amperes). The fundamental is given as a percentage of line current.
1	4.8×10^{-3}	100%	237.71	57%
2	3.1×10^{-3}	2.9 Amperes	4.16	0.04 Amperes
3	1×10^{-3}	5.7	3.22	0.03
4	5×10^{-4}	1.5	2.94	0.004
5	4×10^{-4}	3.4	2.83	0.01

Table 2: Error in measured harmonic current.



(a) (b)

Figure 16: Red Phase Channel Filters - phase response: (a) Voltage, (b) Current.

A.8 Multi-Channel Continuous Real Time Harmonic Monitoring

MULTI CHANNEL CONTINUOUS REAL TIME HARMONIC MONITORING

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Abstract – A multi-channel harmonic monitoring system is described capable of continuous real time processing of harmonic information. Synchronous data acquisition of voltage and current signals is carried out over a predefined integral number of cycles of the fundamental frequency (e.g. 5 cycles). This enables time domain averaging of these signals to an equivalent 'single' cycle of the captured waveform which can then be 'Fast Fourier Transform' analysed with simple rectangular windowing and minimal spectral leakage to provide harmonic data to the 64th harmonic. The system also computes and displays the impedances, active and reactive power, sequence components etc of each harmonic. It is capable of storing harmonic data for more detailed analysis at a later date as well as recording data as a function of any predefined analysis and storage compaction algorithm (e.g. harmonic peak or average values, harmonics exceeding predefined limits etc).

INTRODUCTION

The flow of harmonic currents and their related voltage distortion levels at points of common coupling between consumers is a very complex subject. The consequences of waveform distortion range from slight inconvenience to extreme disruption and therefore legislation to limit distortion levels is being introduced in many power systems [1].

However legislation can only be enforced if adequate 'policing' is available. The main requirements in this respect are the detection of harmonic sources and their interaction with the rest of the power system.

The requirement of real time harmonic analysis, combined with the necessity of computing harmonic components as high as the 50th harmonic, has historically restricted harmonic analyzers to two channels at the most. So to perform a three phase measurement, several of these single phase analyzers must be controlled and synchronized together, the logistics of which is complex, the flexibility limited, and the cost often prohibitive.

Moreover, present limited experience with harmonic measurements in transmission systems indicates that the levels found in the three phases are always different and therefore the simultaneous detection of multiphase information is essential.

The speed of monitoring may not be considered critical in the detection of mainly, steady state waveform distortion. However the possibility of gathering real time information could be used ON-LINE to take instant action upon the detection of unusual levels of non-characteristic harmonics.

This paper describes an harmonic monitoring system which is capable of the continuous acquisition of six or more channels of analogue data, and of computing the Discrete Fourier Transform (DFT) of each channel in real time, to determine each channel's harmonic levels up to the 50th harmonic. The harmonic monitor display incorporates a mouse driven human interface, and this, combined with 'icons' and 'pop-up' menus, enables efficient and user friendly configuration and operation of the monitor.

THE MONITORING ENVIRONMENT

The monitor relies on its connection to the power system to obtain accurate information of the currents and voltages and yet it needs to be adequately isolated from the electrostatic and electromagnetic effects of the high voltage system.

The inputs to the monitor comprise six or more analogue voltages transmitted from transducers by fibre optical cables. These signals are obtained from current and voltage transducers located at appropriate points of the network.

To reduce the signals dynamic range to a level suitable for transmission through fibre optical cables, the fundamental component is attenuated by passing each signal through a highpass filter, with a cut-off frequency at the 2nd harmonic. This leaves the harmonics unattenuated, maintaining them above the noise level. The magnitude and phase change in the signals, introduced by the transducers, interfacing circuitry, and signal conditioning equipment are required to be compensated for in the frequency domain after their DFT's have been computed.

The fibre optical cables provide an effective means of isolation between the high voltage power system equipment, and the signal processing equipment within the monitor.

The original specification for the interface of the monitoring instrumentation and the transducers was made by Electricorp (New Zealand). Such interface and related signal conditioning are illustrated in the schematic diagram of Figure 1.

A diagram illustrating the data flow between the external environment, the operator, and the real time harmonic instrumentation is shown in Figure 2.

STRUCTURE OF THE HARMONIC MONITOR

This section describes the hardware, software, and operation of the harmonic monitor, and discusses the techniques used in applying the DFT to harmonic analysis.

The monitoring system contains three main components: (i) a dedicated signal conditioning and data acquisition system, (ii) a Multibus II multiple processor system, and (iii) an IBM compatible PC-AT. These are illustrated in Figure 3.

The dedicated data acquisition system is designed specifically for the purpose of acquiring six or more analogue voltages simultaneously from external power system transducers and converting them to digital samples suitable for computer processing. Time domain data are converted to harmonic data in the Multibus-II system, and

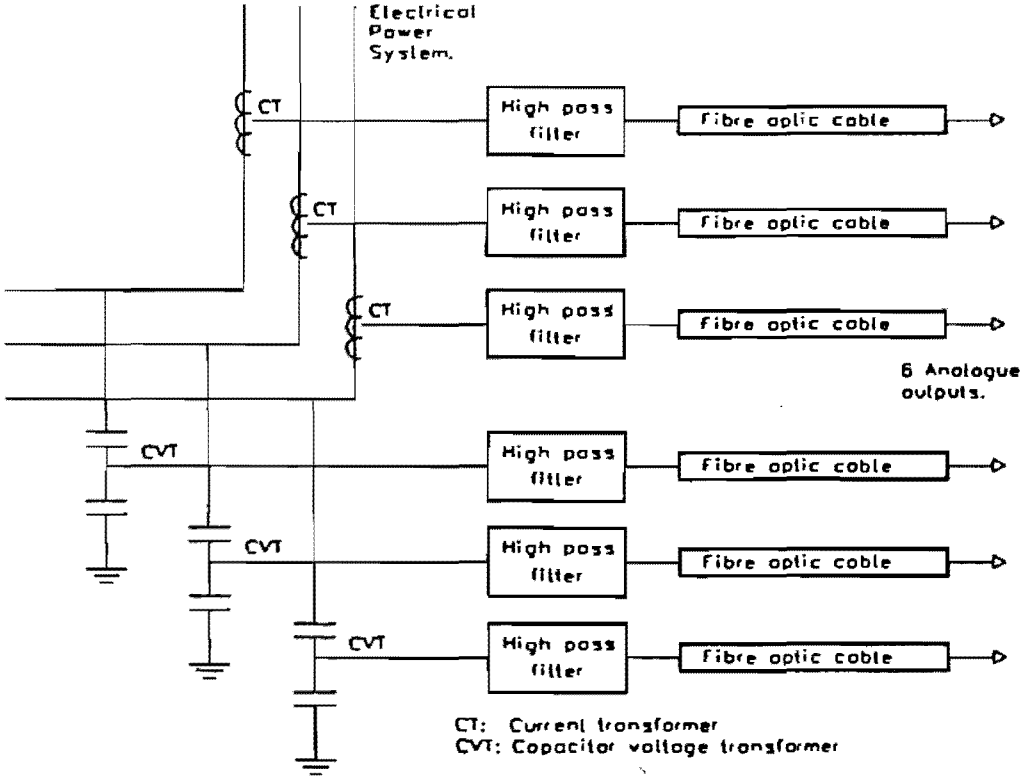


Fig. 1. Electricorp interface and signal conditioning equipment.

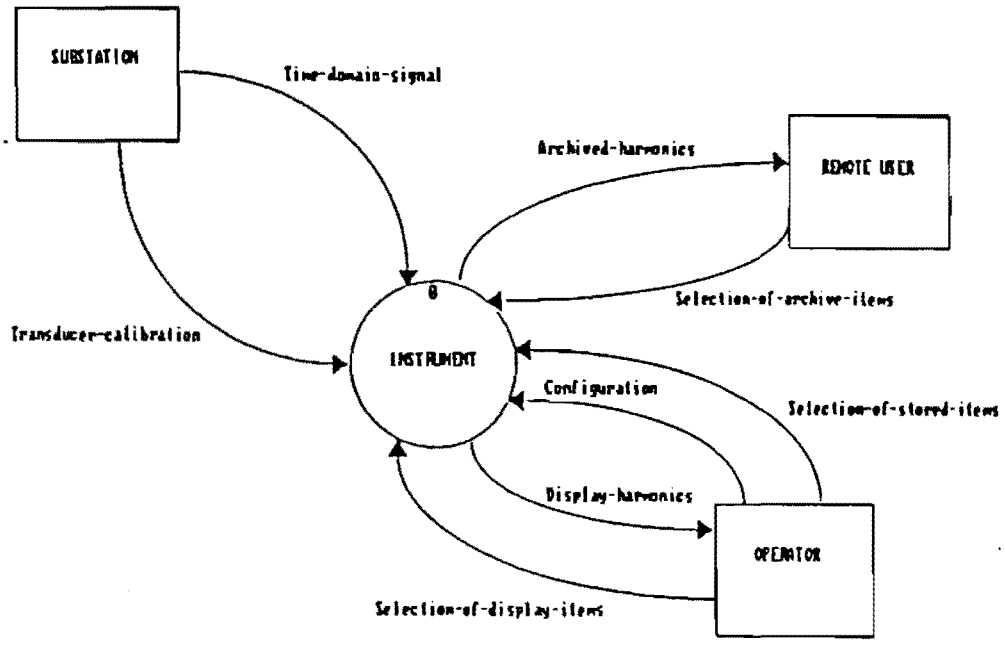


Fig. 2. Data flow diagram.

stored there for later retrieval and analysis. Harmonic data are retrieved and displayed on an IBM compatible PC-AT which is connected to the Multibus II system by a General Purpose Instrumentation Bus (GPIB).

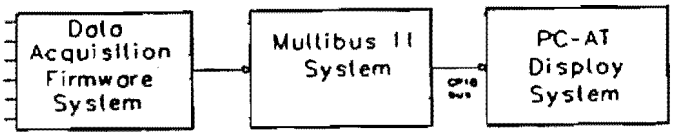


Fig. 3. Structure of the harmonic monitor.

Data Acquisition System

Figure 4 illustrates one channel of the data acquisition system. Each of the inputs fed to the data acquisition system is passed through an anti-aliasing filter. This filter attenuates frequencies above the 50th harmonic to reduce errors caused by aliasing. The signals are sampled and held simultaneously in order to provide time synchronous signals for subsequent sequential analogue to digital conversion, which achieves accurate 12-bit digital representations of the analogue signal.

The sampling signal is produced by the *sample rate multiplier* which has the primary purpose of adjusting the sampling interval in order to maintain it at an 'exact' 1/128 sub multiple of the fundamental period (i.e. accommodate the small changes that may occur in the mains frequency). This device combines an 8751 micro-controller, and a high speed counter (operating at 22MHz), to produce 128 pulses, uniformly spaced in time, within one period of the fundamental. The first sample pulse is locked to the zero crossing of the fundamental waveform. Hence a rectangular window is effectively applied over one period of the fundamental, virtually eliminating the problem of spectral leakage [2][3][4]. The signal conditioning performed to provide the zero crossings of the fundamental waveform is also illustrated in Figure 4.

The output of the analogue to digital converter is a parallel signal which is stored in a first-in-first-out (FIFO) buffer. This provides some buffering between the data acquisition system and the Multibus II system. The data acquisition system also performs an estimate of the fundamental frequency at the time of measurement. This information is transmitted with the digitized signals to the Multibus II system.

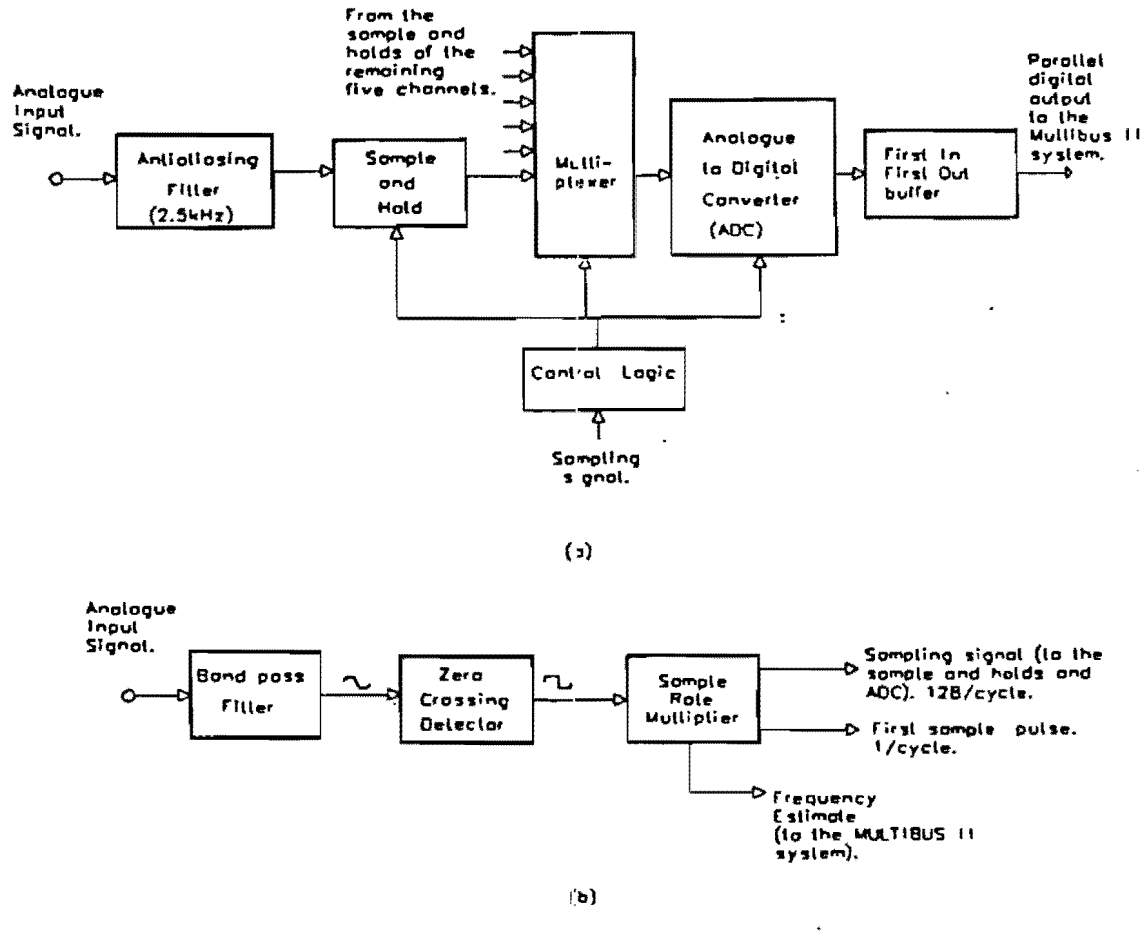


Fig. 4. One channel of the data acquisition system.

The Multibus II System

The data 'captured' in the previous stage still requires considerable transformation to be in a useful form for analysis. It is averaged to reduce computation requirements and the effect of spurious transients, transformed from the time domain to the frequency domain using an FFT algorithm and then processed to store not only the raw harmonic data, but also derived information such as maxima and average levels encountered. Finally the stored data must be made available for further purposes, such as display on the PC/AT, or control purposes designed to reduce the detected harmonic levels.

A system which provides a parallel processing environment, such as Multibus II enables the separation of the processing requirements into three main parts, with each part performed by a separate single board computer, as illustrated in Figure 5.

The Acquisition Processor

Information from the data acquisition system passes directly to the memory of the first board in the Multibus II system – the acquisition processor board. This is a stand alone board (it does not run any operating system) and is based on an 80186 microprocessor.

Each of the channels of time domain data is averaged over five consecutive cycles of the fundamental component. This reduces the 'picket fence effect' by narrowing the frequency bins centred on each harmonic [1][4].

Alternatively, the picket fence effect can be reduced by broadening the time domain truncation interval (by sampling over five periods of the fundamental for instance), which effectively narrows the harmonic frequency bins (the time scaling property of the Fourier transform). This would, however, involve the processing of significantly more data. Sampling over 5 cycles, instead of one, increases the frequency resolution of the monitor, transforming it from the desired harmonic analyser into a more general spectrum analyser. Resolving frequencies between harmonics is seen as a waste of processing power in this application.

The averaged data are formed into packets, which are queued by the acquisition processor, ready for passing to the FFT processor via the Multibus II message passing system.

When initialized the board runs a series of tests under a 'Built In Self Test' (BIST) module. It then loads the application program to be run from the master CPU board running under the RMX286 operating system. This application when loaded initializes the board hardware, creates queues for data entering the MBII system from the data acquisition system, averages the incoming data over five cycles, and stores the data in queues ready to be sent to the FFT processing board.

Interrupt routines are created to handle the incoming data and to send the data via solicited messages to the next board. Direct Memory Access (DMA) devices handle the bulk of the data transfer on and off the board. The code is written in PLM/86 high level programming language with a small amount of assembler used in initialization stages.

The source code is written in separately compiled modules with their own initialization structures allowing each task to be managed effectively. Modules have been created for message passing, queue control, acquisition and averaging etc.

The FFT Processor

Based on an 80386 microprocessor, this stand alone board uses a radix-2 FFT algorithm to compute the DFT of the averaged time domain data received from the acquisition processor. The requirement that the data be transformed in real time ultimately restricts the number of channels that can be handled by this board.

The output data packets from the FFT algorithm are queued ready for message passing to the compaction and storage board.

This 386 board is running in its 8086 mode which maximizes its processing capabilities. It also runs a BIST and then loads its application from the master CPU. The application initializes the board and then creates queues for averaged data to arrive from the data acquisition board and queues for FFT data to go to the main CPU board. Interrupt service routines and DMA transfer routines service the reception and transfer of data from the acquisition board and to the main CPU.

The software is written in PLM/86 and ASM86, as a set of modules. The data arrives from the data acquisition board at intervals of five cycles of the fundamental frequency (e.g. 100 mS for 50 Hz). The software receives a message of time-domain-averaged sample packets, applies the FFT algorithm to each of the packets, and then sends the data to the next board.

To achieve this task the FFT algorithm has been written in PLM/86 and then hand optimized in assembler. The resulting algorithm including all message passing takes typically 80 percent of the processing power of this board.

The Compaction and Storage Processor

To enable the inspection of harmonic levels at a later time, or at a location other than in the field, the harmonic data are compacted and stored on a hard disk drive.

The Compaction and Storage process takes data from the FFT processing board and compacts it by both averaging over an interval of time, and by selecting the maxima over the same interval. This is done for each step of one second, ten seconds, one minute, ten minutes, and one hour. At each step both options are chosen leading to a tree structure of available data items (see Figure 6). The time stamp from the corresponding time domain source data is appended to every FFT packet, enabling the precise identification of the time of measurement of the raw data.

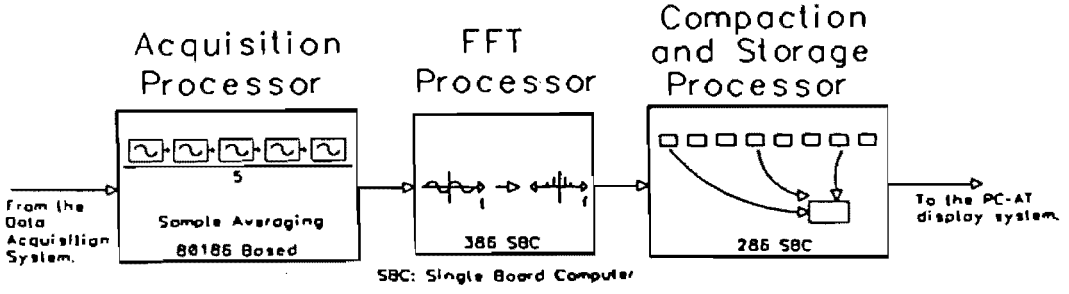


Fig. 5. The three main functions performed by the Multibus II system boards.

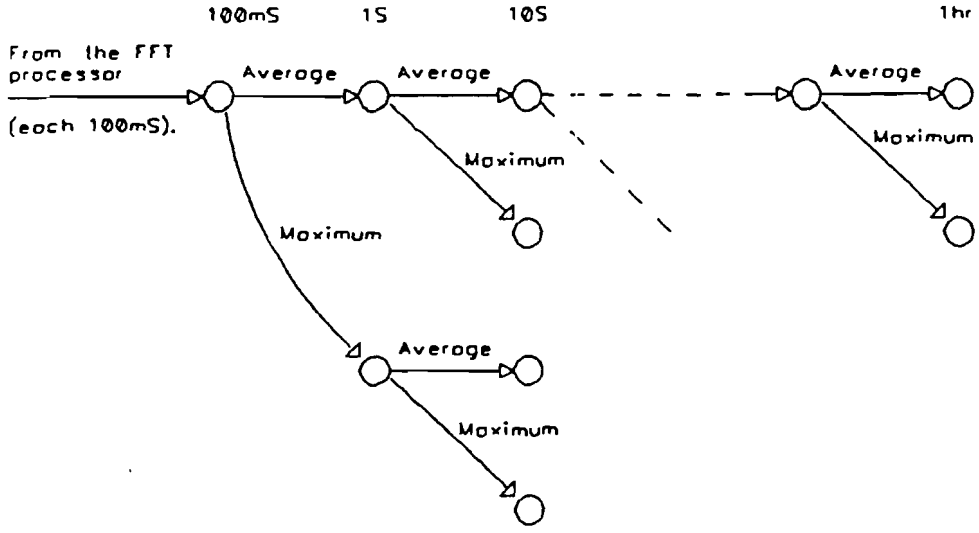


Fig. 6. Compaction algorithm.

Each of these nodes of data items is then stored in a arate file, the collection of files making one set of adings. Future expansion will include the ability to provide for different algorithms (apart from averaging and maxima) at each step of the tree. This will also require an ability to select only some nodes to keep storage requirements within reasonable bounds.

The board is based on the 80286 processor and is the master cpu in the Multibus II chassis, running the RMX-II operating system. This board starts by running the system debugger which is used to boot the operating system from disk. The board then downloads the applications to each of the acquisition and FFT processors. After login the user is able to start either or both of two main applications 'Compaction and Storage' and 'Retrieval and Replay' (documented below).

The Retrieval and Replay Task

The 'set of readings', stored on disk, may be required for display and/or further analysis. The retrieval task reads the data items selected back into memory and sends them via a GPIB interface to the PC/AT.

The Intel RMX286 real-time multi-tasking operating system allows more than one task to be executed in the same board, and so the retrieval is also performed on the master cpu of the Multibus system but at a lower priority than the compaction. The two tasks are started from completely separate logins, which allows the instrument to be recording one 'set of readings' while displaying a completely separate 'set of readings' from another occasion. The monitor will also display in real time the same 'set of readings' as is being recorded.

In addition to compaction and storage, this board sends data over a GPIB bus to the PC/AT for display and also acts as a control centre to which other boards report exceptions if and when they occur. These multiple tasks are handled very efficiently by the RMX running on this board.

The algorithms for the replay (and the compaction) are written in PLM/286 and rely heavily on the multi-tasking operating system RMX-II for aspects of priority, message passing (from the FFT processor), file storage and retrieval. The code for interfacing to the GPIB were written and tested locally. Each section of code is written as a separate module, which aids the maintenance of complex programs.

The PC/AT Display

Perhaps the most important feature of an instrument such as this is the human interface. The way data are presented to a user is tremendously important to his or her cognition of the results. The ease with which the system may be configured to perform the desired operations ultimately determines its popularity, and is conducive to its correct use.

The user interface to this instrument is mouse driven and uses icons (graphically drawn keys) to provide a very comprehensible instrument interface.

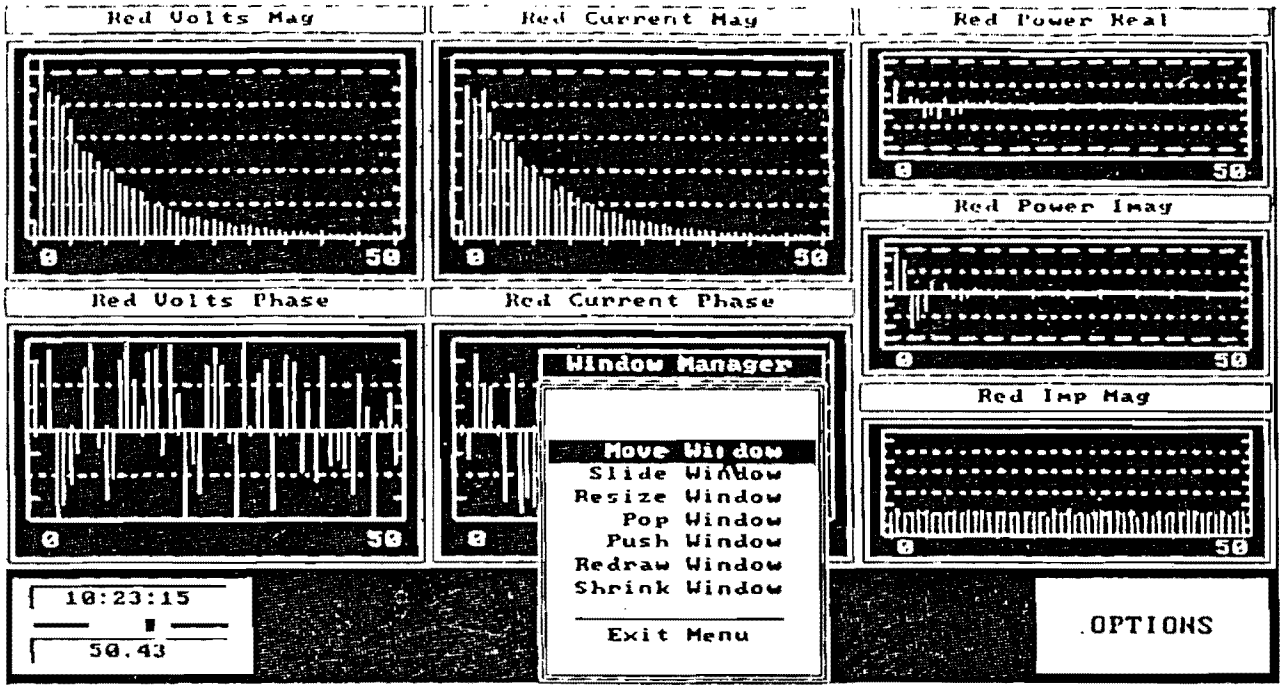
Data are displayed as graphs of harmonic voltage, current, impedance, and power against harmonic order. Both the magnitude and phase of these variables can be displayed. Each graph is contained in a separate window, and the windowing system enables a user to layout the display to suit his or her particular requirements. This is achieved by enabling a user to move a window about on the display, shrink or enlarge it, and/or to completely remove it.

In addition to the graphs, the absolute fundamental frequency is shown on the display, and an indication of whether or not it is within the prescribed limits is also shown.

The PC/AT software is written exclusively in MODULA-2. MODULA-2 has *multi-tasking* built into the language which permits the writing of a *scheduler* for concurrently executing tasks or processes. The scheduler uses message passing as its only method of synchronization. The use of the scheduler permits further decomposition of the PC/AT software into tasks even though PC-DOS itself does not allow multi-tasking. The scheduler takes care not to allow the interruption of tasks that are using PC-DOS operating system calls; this may cause corruption of the operating system as many PC-DOS calls are not re-entrant.

EXAMPLES OF DISPLAY

is an example of the information that may by the operator of the *Harmonic Analyser*. left is a small window showing the undamental frequency (50.43 Hz) and the At the lower centre is a *window manager* s been activated by *clicking* the mouse in



the window to be changed. Options for controlling the *Harmonic Analyser* are obtained by *clicking* the mouse in the *options* box at the lower right. The display windows themselves show voltage, current, power and impedance of a test waveform (square wave) for the red phase only. The displays are updated once a second.

CONCLUSIONS

The Multibus II multiprocessing computer system provides a suitable environment for continuous real time analysis and monitoring of the three-phase power system.

Software has been developed to provide the type of information required by current legislation but any special present or future requirements can be easily accommodated without altering the hardware structure. Highly modular software has been used throughout which is easy to correct and expand because it is easier to understand.

In each application the instrument should be calibrated prior to the measurements to account for phase errors introduced by analogue devices such as transducers and anti-aliasing filters. The proposed system can also become an important part of state estimation and ON-LINE power system control in the future.

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Charles B. Lake was born in New Zealand on April 5th 1956. He graduated BE (Hons) in 1976 and ME in 1977 at Canterbury University, New Zealand. He has worked in postgraduate studies on HVDC convertor controllers and as a Research Engineer for Taito NZ Ltd training engineers and computer scientists in aspects of software development. In 1982 he worked as design engineer with Microage (NZ) Ltd developing systems, circuits and software for use in Electronics Point Of Sale (EPOS) equipment, eventually becoming a director of this company. In 1987 he took a position as lecturer in the Electrical and Electronic Engineering department of the University of Canterbury, New Zealand. Recent research interests include HVDC control systems and harmonic measurement instrumentation.

Michael B. Dewe was born in Singapore on August 28, 1940. He graduated in 1964 in Electrical Engineering at the University of Cape Town from where he proceeded as Commonwealth Scholar to the University of Canterbury, New Zealand completing research studies for an M.Eng. degree in 1966. He then joined the Space Division of Hawker Siddeley Dynamics Ltd (now British Aerospace) where he became Group Leader of Electronic Systems Design. In 1973 he took up a Lectureship in Electrical Engineering at the University of the Witwatersrand, South Africa, where as Senior Lecturer he was responsible for Control research and teaching activities. He accepted a Senior Lectureship in the Electrical and Electronic Engineering Department of the University of Canterbury in 1978 working on electronic, digital and control applications in the Power Systems field. In 1981 he joined Wormald Vigilant Ltd, a New Zealand company of the Wormald International Group involved in fire and security alarms, building services, SCADA systems and industrial control. He became Engineering Manager and Associate Director of this company before rejoining the Electrical and Electronic Engineering Department of the University of Canterbury in his present post as Senior Lecturer in 1985. Recent research activities include the development of harmonic measurement systems, domestic energy management and the development of transformer insulation condition monitoring equipment.

Alan J.V. Miller was born in Hokitika, New Zealand in 1966. He graduated in 1988 with a BE (Hons) degree in Electrical and Electronic Engineering at the University of Canterbury. He is currently pursuing postgraduate research into real time measurement of Power System harmonics leading to a PhD degree at the University of Canterbury.

Mike Shurety was born in London, England in 1949. He moved to New Zealand with his family in 1961. He has worked in electronics and computers in New Zealand for twenty years. Nine years of which have been spent in the Electrical and Electronic Engineering Department of the University of Canterbury, four years at Lincoln College, and the remainder in industry. For the last three years he has been employed as a System Analyst in the Department of Electrical and Electronic Engineering of the University of Canterbury and has just been appointed Computer Manager in the same department.

Michael J. Cusdin joined the Electrical and Electronic Engineering Department of the University of Canterbury, New Zealand, in 1970 as a Senior Technician after 9 years in the Royal New Zealand Airforce as a Radio Technician. In 1975 he obtained the New Zealand Certificate in Applied Electronics after 4 years part-time study at the Christchurch Polytech Institute. He has contributed to the Electrical and Electronic Engineering Department's research in developing several types of sonar systems that operate in air, water and body tissue. He is also assisting staff and postgraduate students in the running of various Intel Multibus based computer systems. He is currently a Senior Technical Officer in the Electrical and Electronic Engineering Department and is responsible for the development of the front end data acquisition hardware for the Harmonic Analysis System.

Jos Arrillaga received the BE degree in Spain and the MSc, PhD, and DSc in Manchester, where he led the power systems group of UMIST between 1970–74. He has been a Professor at the University of Canterbury since 1975. He is a Fellow of the IEE, of the New Zealand Institution of Engineers and of the Royal Society of New Zealand.

A.9 Object Oriented Message Passing Software in CHART I

OBJECT ORIENTED MESSAGE PASSING SOFTWARE FOR A THREE PHASE REAL TIME HARMONIC MONITOR.

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Abstract.

This paper discusses the design and implementation of a software system that comprises the operating environment for a six channel harmonic analyser. The software system is designed to average, analyse, compact, store and display harmonic data in real-time. Particular emphasis is placed on *Object Oriented* and *Message Passing* aspects that enhance the maintainability of the software.

1 Background To The Harmonic Analyser.

In September 1985 the New Zealand Ministry of Energy produced a specification for a real-time harmonic analyser [1] [2]. The Electrical and Electronic Engineering Department of the University of Canterbury undertook to develop such a system.

The desire to measure the harmonic content in power systems stems from several sources. There is the need to monitor and regulate the harmonic content of the power supply system, in order that levels set to protect users of the system, and the system itself, are adhered to. Another stems from the desire to verify that the harmonic content, as predicted by research, is indeed correct. Knowledge of harmonic content is also valuable when determining the required rating of new devices within the system - devices such as power factor correction capacitors.

For a fuller discussion on Harmonic Analysis refer to "A Six Channel Real Time Harmonic Monitor" [10].

2 The Harmonic Analyser Hardware.

The Harmonic Analyser hardware comprises an Intel Multibus II system and a PC/AT clone connected together with a GPIB parallel interface. The Multibus II system samples the the six input channels concurrently, extracts the harmonic information and transfers it to the AT for display.

2.1 The Multibus II System.

The Mutibus II system comprises three processor boards, some permanent storage media and some custom hardware for sampling the six input channels. The custom hardware samples the six channels and passes the data through a DMA (Direct Memory Access) channel to the first processor (an Intel 80186). This processor averages five cycles of the time domain signal and passes it via the Multibus II bus to the FFT (Fast Fourier Transform) [4] processor (an Intel 80286). This processor performs the FFT on all channels and passes the frequency domain data to the third processor (also an 80286) which compacts and stores the data to disk. The third processor also sends the data via the GPIB (General Purpose Instrument Bus) interface to the PC/AT clone for display.

2.2 The IBM PC/AT Clone.

The PC/AT clone receives the frequency domain data packets over the GPIB bus from the Multibus II system. After suitable scaling the spectra are displayed in user definable windows on the AT's screen. Magnitude and phase of voltage and current are displayed for each of the six channels. A friendly window and mouse (WIMPS) operating environment is employed to enable technicians and engineers to access the system easily.

3 The Need for Effective Programming Techniques.

To properly maintain software one must first understand it. This is not usually so much of a problem for the original author but will be for those who are to continue development. Good documentation is the first step in ensuring that those that follow on will understand, but due to time pressures it is often not done till the end of the project. Documentation on its own is not enough to ensure maintainablity. It is necessary to break the program into smaller self contained *modules* so that these may be studied in isolation. This is known as *increasing modularity*.

Increasing modularity also prevents *module dependancy* which manifests itself as problems in one module caused by some programming change in another. This is often caused by indiscriminate use of *global variables* especially in languages where variables do not have to be declared before use (e.g. FORTRAN 77 and BASIC). The program may be further sub-divided into tasks or processes which perform specific functions. These processes or tasks may exchange information.

4 Object Oriented Programming.

The term *object* has been in use in many fields of computer science since the early 1970's to refer to ideas that seem to be completely unrelated. All of these concepts appear to have been invented to manage the increasing complexity of computer software. Each is an attempt to represent components of a modularly decomposed system or unit of knowledge representation. Some of these concepts are:

- *abstract data types* in programming languages such as MODULA-2 and Ada [11].
- units of information with *class/instance* and *super-class/sub-class* hierachies as in Simula and Smalltalk [5].
- computational units that carry out actions in response received messages called *actors* in languages like Act and ABCL/1 [6] [9].
- modules or units for knowledge, such as *frames*. [8]
- operating system resources (e.g. Intel's RMX).

The common characteristic is that of an entity in the computing domain which is *self-contained* and has a *consistent communication protocol*. Objects may not be operated on directly but only by using provided procedures or by asking the object to perform operations on *itself*.

Object oriented programming is a style that has developed in the last ten to fifteen years and is mainly due to the influence of *Smalltalk* and other less well known *object oriented languages*. The concept we have used in our software is that of an *object* which contains as part of its data structure the *methods* which are procedures for performing operations on these data structures. The methods are executed in response to *messages* sent to the object by other objects in the programming environment. Here a message has the same semantics as a procedure call.

This means procedures and functions which *operate* on the object are carried around by the object. Central to this concept is the idea of *inheritance*. Inheritance allows the programmer to *extend* previously declared structured data types. Object oriented programming is concerned with *abstraction* not only of data types but also of all of the entities which occur in the domain of computing. An object is a dynamic instance of a general class.

Some of the newer procedural languages are beginning to use some of these ideas.

- C++
- MODULA-3
- Object Pascal

Luckily much of the utility of *objects* can be obtained without the special programming languages by the use of ordinary record structures and procedure variables. *Object oriented* can also mean the construction of *modules* which contain only the object and its procedures and functions. Since inheritance is normally provided by the compiler it must be simulated by nesting records. With programmer discipline many ordinary procedural languages can use these techniques.

4.1 Message Passing.

Message passing used here should not be confused with the notion of message passing in the discussion of objects in the previous section. Whilst related, message passing in the domain of objects can have the same semantics as an ordinary procedure call. Here *message passing* [7] is a technique by which multiple processes or tasks running on one processor or on many processors exchange information and synchronise themselves. In the code, explicit calls to procedures called *send* and *receive* are used. Synchronisation is necessary to control the timing of information exchange and to control the proper order of process execution.

Message passing is not the only way of synchronising the execution of parallel and pseudo parallel processes but does have a certain elegance. The most common forms are:

- binary or counting semophores.
- shared memory flags.
- message passing.

To exchange data some common methods used are

- shared memory areas.
- message passing.

One advantage of using message passing is that local copies are available to concurrent processes allowing exclusive use of the data in the message. Message passing achieves synchronisation and data exchange at the same time. Messages are sent between processes *synchronously* or *asynchronously*.

4.1.1 Synchronous Communication.

In synchronous communication two schemes are used.

1. The sender is suspended until the receiver takes the message before continuing execution.
2. The sender is suspended until the receiver waits for the next message before continuing execution.

These techniques provide what is sometimes called *tightly coupled* processes. Method 2 above is useful for excluding access to common resources, since the two processes operate sequentially.

4.1.2 Asynchronous Communication.

In asynchronous communication the receiver waits as in synchronous communication but the sender never waits. The sender places its message in a queue and continues execution immediately. This allows messages to be sent by interrupt service routines, which because of critical timing must not be held up. This method also allows processes running on separate processors to operate in true parallel.

4.2 Object Oriented Programming Example.

Our example program (See Figure 1.) calls *InitQueue* to create an instance of the object *QUEUE*. It then calls *InsertInQueue* to add some data to the queue. If there is an error then a message is printed, otherwise processing continues.

The *DEFINITION* of the module *Queue* (See Figure 2.) shows the types and procedures visible to the user program. All identifiers declared here are available to any program wishing to *IMPORT* them.

The *IMPLEMENTATION* of the module *Queue* (See Figure 3.) shows the hidden *QUEUE* object and the code used to initialise the *methods* for manipulating the QUEUE.

Notice:

- the *InitQueue* procedure assigns the procedures that do the inserting and removing etc. to the procedure variables in the *QueueInfo* record, according to the *QUEUETYPE*.

- the *InsertInQueue* procedure calls the *Insert* field of the *QueueInfo* record to do the actual insertion

The advantages of this approach are:

- the *QUEUE* data structure cannot be tampered with by the user program
- the procedures for manipulating the *QUEUE* are carried around by the instance of the *QUEUE* object
- The decision branch for deciding which sort of queue we are dealing with is in the initialisation code. If the *insert* is in a hot loop we are saving time.

5 The Harmonic Analyser Software.

The software will be dealt with in two sections.

- PL/M software for the Multibus II system.
- MODULA-2 software for the PC/AT

5.1 The Multibus II Software.

The Multibus II software is written primarily in PL/M. The programming environment runs under Intel's operating system RMX. RMX is a real-time multi-tasking operating system which itself contains the concept of objects. In RMX objects are processes, mail boxes, data segments etc and may be catalogued and retrieved by completely separate parts of the software, by specifying the ascii name of the object.

Whilst the choice of PL/M as a programming language would seem to make a mockery of some of the earlier discussion, the software can still make use of many of the ideas we have discussed. In particular the software is *object oriented* in that data types are worked on only by procedures provided for the purpose and is decomposed into a set of concurrently executing tasks. These tasks synchronise and exchange data using RMX operating system calls to send and receive messages through mail boxes. Modules using this scheme are unaware of whether they are sending to processes on the same processor board or not.

PL/M provides no method for enforcing this programming style and so it must be achieved by agreement of all programmers on the team. Since the team was small and geographical distances between members also small this was not a problem.

Data types and related procedures declarations are placed in one header file which is *included* into the main program that uses the module. All modules declare an initialisation procedure with a standard format (*modulename*$initialisation) to be called before any other procedures in the module. These initialisation procedures may be called any number of times but will only execute once. This is so that users of the module do not need to know if another module has called the initialisation procedure or not. The implementation of the code is independently compiled and is in a separate file.

One particularly nice feature of the Multibus II system hardware is that multiple processors on the system bus communicate with each other through message passing rather than the traditional hardware handshaking lines. The message passing between processor boards is controlled by a *message passing co-processor* (MPC) which every board must have to communicate. This allows us to have a unified message passing structure in both hardware and software. The format of messages passed around the system both on the Multibus II system, across the GPIB bus and internally between processes on the PC/AT are the same. This gives us a *global message space*, a concept which greatly eases the construction and addition of new software modules.

5.2 The PC/AT Software.

The PC/AT software is written exclusively in MODULA-2. In direct contrast to the PL/M software mentioned above MODULA-2 provides *opaque* or *hidden* data types. This provides protection at the compiler level of data structures declared to be opaque. Opaque data types is a mechanism for hiding the implementation details of the data type. The user of the module may declare variables of the opaque type but can not operate on its hidden structure.

MODULA-2 also has *multi-tasking* built into the language which allowed us to write a *scheduler* for concurrently executing tasks or processes. The scheduler uses message passing as its only method of synchronisation. The use of the scheduler allowed us to further decompose the PC/AT software into processes even though PC-DOS itself does not allow multi-tasking. The scheduler takes care not to allow the interruption of processes that are using PC-DOS operating system calls as this may cause corruption of the operating system due to many PC-DOS calls not being re-entrant.

The main body of the software is a window oriented *user interface* which allows windows to be defined and manipulated on the screen. The windows are objects which contain *methods* that the window manager can invoke to control the window environment. These methods include procedures to re-draw the window when an exposure event occurs.

6 Conclusion.

Experience has shown that the use of these techniques leads to the development of highly modular software, which is easier to correct and expand because it is easier to understand.

Acknowledgement.

The authors are grateful of the financial support offered by the Electricity Corporation of New Zealand and the Power Systems Group of the Electrical Engineering Department for the development of this instrument. A.J.V. Miller acknowledges the award of a University Grants Committee postgraduate scholarship, and we thank Professor J. Arrillaga for his interest in this project.

Figure 1: User Code for Object Oriented Programming Example.

```
PROCEDURE Demo;
CONST
  Max = 100;
VAR
  MyQ : QUEUE;
BEGIN
  MyQ := InitQueue(Queue, Max);
  IF InsertInQueue(MyQ, MyData, SIZE(MyData)) THEN
    (* Insert successful so continue *)
    .
    .
  ELSE
    (* queue probably full *)
    WriteErrorMessage('Queue full');
    HALT;
  END;
  DoSomething(MyQ);


END Demo;
```

Figure 2: Definition for Object Oriented Programming Example.

```
DEFINITION MODULE Queue;

TYPE
  QUEUETYPE = (Stack, Queue); (* Stack = FILO, Queue = FIFO *)
  QUEUE;                      (* Implementation of QUEUE hidden from user *)


  PROCEDURE InitQueue(qt : QUEUETYPE; MaxEntries : CARDINAL) : QUEUE;

  PROCEDURE InsertInQueue(q    : QUEUE;
                          data : ADDRESS;
                          len  : CARDINAL) : BOOLEAN;

  PROCEDURE RemoveFromQueue(q       : QUEUE;
                            data    : ADDRESS;
                            VAR len : CARDINAL) : BOOLEAN;

  PROCEDURE ReadNthElement(q       : QUEUE;
                           elno    : CARDINAL;
                           data    : ADDRESS;
                           VAR len : CARDINAL) : BOOLEAN;

  PROCEDURE MaxQueueSize(q : QUEUE) : CARDINAL;

  PROCEDURE QueueEntries(q : QUEUE) : CARDINAL;

  PROCEDURE DeleteQueue(VAR q : QUEUE);

  PROCEDURE FlushQueue(q : QUEUE);

END Queue.
```

Figure 3: Implementation for Object Oriented Programming Example.

```
IMPLEMENTATION MODULE Queue;

TYPE

  QUEUE = POINTER TO QueueInfo;

  QUEUEIPROC = PROCEDURE(QUEUE, ADDRESS, CARDINAL) : BOOLEAN;

  QUEUERPROC = PROCEDURE(QUEUE, ADDRESS, VAR CARDINAL) : BOOLEAN;

  QUEUENPROC = PROCEDURE(QUEUE, CARDINAL, ADDRESS, VAR CARDINAL);

  QueueInfo = RECORD
    Latest   : QUEUEPTR;   (* POINTER to linked list of data elements*)
    Insert   : QUEUEIPROC; (* PROCEDURE variable for inserting *)
    Remove   : QUEUERPROC; (* PROCEDURE variable for removing  *)
    ReadN    : QUEUENPROC; (* PROCEDURE variable for reading nth element *)
    MaxEnt   : CARDINAL;
    NumEnt   : CARDINAL;
  END;
  .
  .
  .
  PROCEDURE InitQueue(        qt : QUEUETYPE;
                      MaxEntries : CARDINAL) : QUEUE;
  VAR
    q : QUEUE;
  BEGIN
    ALLOCATE(q, SIZE(q^));
    WITH q^ DO
      MaxEnt := MaxEntries;
      NumEnt := 0;
      Latest := NIL;
      CASE qt OF
        Queue :
          Insert := InsertQueue; (* Initialise PROCEDURE variables *)
          Remove := RemoveQueue; (* with actual procedure names *)
          ReadN  := ReadNQueue;  (* according to queue type *)
      | Stack :
          Insert := InsertStack;
          Remove := RemoveStack;
          ReadN  := ReadNStack;
      END;
    END;
    RETURN q;
  END InitQueue;
  .
  .
  .
  PROCEDURE InsertInQueue(   q : QUEUE;
                          data : ADDRESS;
                           len : CARDINAL) : BOOLEAN;
  BEGIN
    RETURN q^.Insert(q, data, len); (* PROCEDURE variable 'called' *)
  END InsertInQueue;
```

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A.10 A Six Channel Real Time Harmonic Monitor

A Six Channel Real Time Harmonic Monitor

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Abstract

Harmonic monitoring is essential in modern power system planning and operation, whether it be for isolation of harmonic sources, assessment of compliance to harmonic legislation, or research - to verify computer simulations.

A portable six channel real time harmonic monitor is presented. The harmonic monitor is capable of acquiring six analogue voltages, averaging over five cycles of the 50 Hz fundamental component, computing the discrete Fourier transform of the averaged data up to the 50th harmonic, and displaying voltage and current magnitudes and phases in real time. Moreover, the real time harmonic monitor also computes and displays harmonic impedance and power, and is capable of storing harmonic data for analysis at a later date, or harmonic data that corresponds to certain peaks that may occur while monitoring.

1 INTRODUCTION

The use of highly non-linear power electronic devices in power systems results in some distortion of power system waveforms from their ideal sinusoidal shapes. The expanding use and size of these devices, means that the waveform distortion they cause is of such a level that it has a significant effect on power system operation.

The most apparent consequence of this power system waveform distortion is interference with communication circuits - by induced currents of audible frequency in communication lines. While this is obviously undesirable, waveform distortion may have less obvious, but nevertheless very detrimental, effects on power system equipment. The maloperation of crucial protection equipment, or the overloading of power apparatus, are just two instances in which waveform distortion can create power system operation problems.

Waveform distortion must be contained to acceptable levels to avoid these problems, and New Zealand legislation provides these levels in the "Limitation of Harmonic Levels Notice",. 1981 [1]. For example, the limit of the 3rd harmonic voltage at a point of common coupling[1] for a nominal system voltage of 66kV or above is 2.3 percent of the nominal phase-to-earth system voltage. The current limit of the 3rd harmonic at a nominal system voltage of 66kV is 1.7 Amperes. The outstanding problem then, is to provide some reliable means of measuring waveform distortion, and of finding its source.

1.1 Harmonic Analysis

As power system waveforms are generally periodic in nature, it is convenient to analyse them using the Fourier Series, where the distorted waveform is considered to consist of a fundamental sinusoidal component, with a series of higher order harmonic components, at frequencies which are integer multiples of the fundamental frequency [3].

Harmonic analysis is the process of calculating the magnitudes and phases of the fundamental and higher order harmonics of the periodic waveform. The harmonic levels offer some measure of waveform distortion. Moreover, the phases of harmonic voltage and current give an indication of the direction of harmonic power flow, and combined with voltage and current magnitudes, enable the calculation of harmonic power and impedance. The fundamental phase provides a common phase reference for the harmonics, thereby enabling the calculation of the original voltage and current waveforms.

[1] A point of common coupling is that busbar electrically closest to any consumer through which any current must flow to that consumer and one or more other customers.

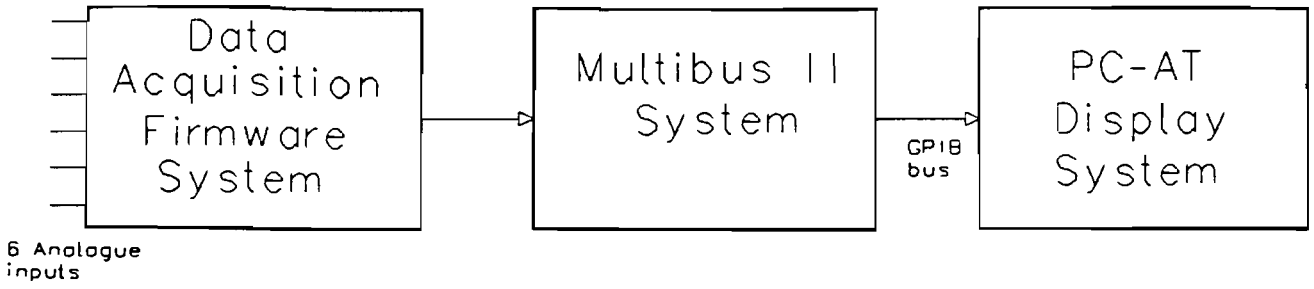

Figure 1: The complete harmonic monitor.

1.2 Harmonic Analysers

The requirement of real time harmonic analysis, combined with the necessity of computing harmonic components as high as the 50th harmonic, has historically restricted harmonic analysers to two channels at the most. So to perform a three phase measurement, several of these single phase analysers must be controlled and synchronised together, the logistics of which is complex, and the cost often prohibitive. For instance, the Electricity Corporation of New Zealand uses three Wandel and Golterman NOWA-1 Power line Harmonic Analysers controlled by an IMB PC XT.

This paper discusses a portable harmonic monitor which is capable of the continuous acquisition of six channels of analogue data, and of computing the Discrete Fourier Transform (DFT) of each channel in real time, to determine each channel's harmonic levels up to the 50th harmonic. The harmonic monitor display incorporates a mouse driven Human interface, and this, combined with 'icons' and 'pop-up' menus, enables efficient and user friendly configuration and operation of the monitor. The specification for this harmonic monitor was issued by the then Electricity Division of the Ministry of Energy in 1986 [2].

2 THE HARMONIC MONITOR

The harmonic monitor is based on a Multibus II multiple processor system, with a dedicated data acquisition firmware system, designed specifically for the purpose of acquiring six analogue voltages, obtained from power system transducers. Harmonic data are displayed on an IBM compatible PC-AT, connected to the Multibus II system by a General Purpose Instrumentation Bus (GPIB). The complete system is illustrated in Figure 1. This section describes the hardware and operation of the harmonic monitor, and discusses the techniques used in applying the DFT to harmonic analysis. A discussion of the techniques used in the software system is given by M.R. Shurety, in the paper "Object Oriented Message Passing Software for a Three Phase Real Time Harmonic Monitor" [4].

2.1 The Data Acquisition Firmware System

The inputs to the data acquisition firmware comprise six analogue voltages, transmitted from the transducers by fibre optical cables. These six signals are obtained from current and capacitive voltage transformers, located at appropriate points on a busbar. To reduce the signals' dynamic range to a level suitable for transmission through fibre optical cables, the fundamental component is attenuated by passing each signal through a highpass filter, with a cut-off frequency of 100Hz.[2] This leaves the harmonics unattenuated, maintaining them above the noise level. The magnitude and phase change in the signals, introduced by the highpass filters, are compensated for in the frequency domain after their DFT's have been computed. The fibre optical cables provide an effective means of isolation between the high voltage power system equipment, and the digital signal processing equipment. The signal conditioning equipment and data acquisition firmware are illustrated in Figure 2(a).

As shown in Figure 2(b), each of the six inputs to the data acquisition system are passed through an optical isolator. This provides an extra degree of isolation from the power system, as well as isolating earths between Electricorp equipment and the data acquisition firmware. Anti aliasing filters attenuate frequencies above the 50th harmonic (2.5kHz) to reduce errors caused by aliasing. The six signals are sampled simultaneously in order to provide a constant signal to the analogue to digital converters (ADC's), which achieve an accurate 14 bit digital representation of the analogue signal.

[2]The current and voltage transformers are owned by the Electricity Corporation of New Zealand, and are permanently installed in New Zealand Sub Stations. The highpass filters and fibre optic cables are supplied by ASEA, and are intended for use as part of this measurement system.

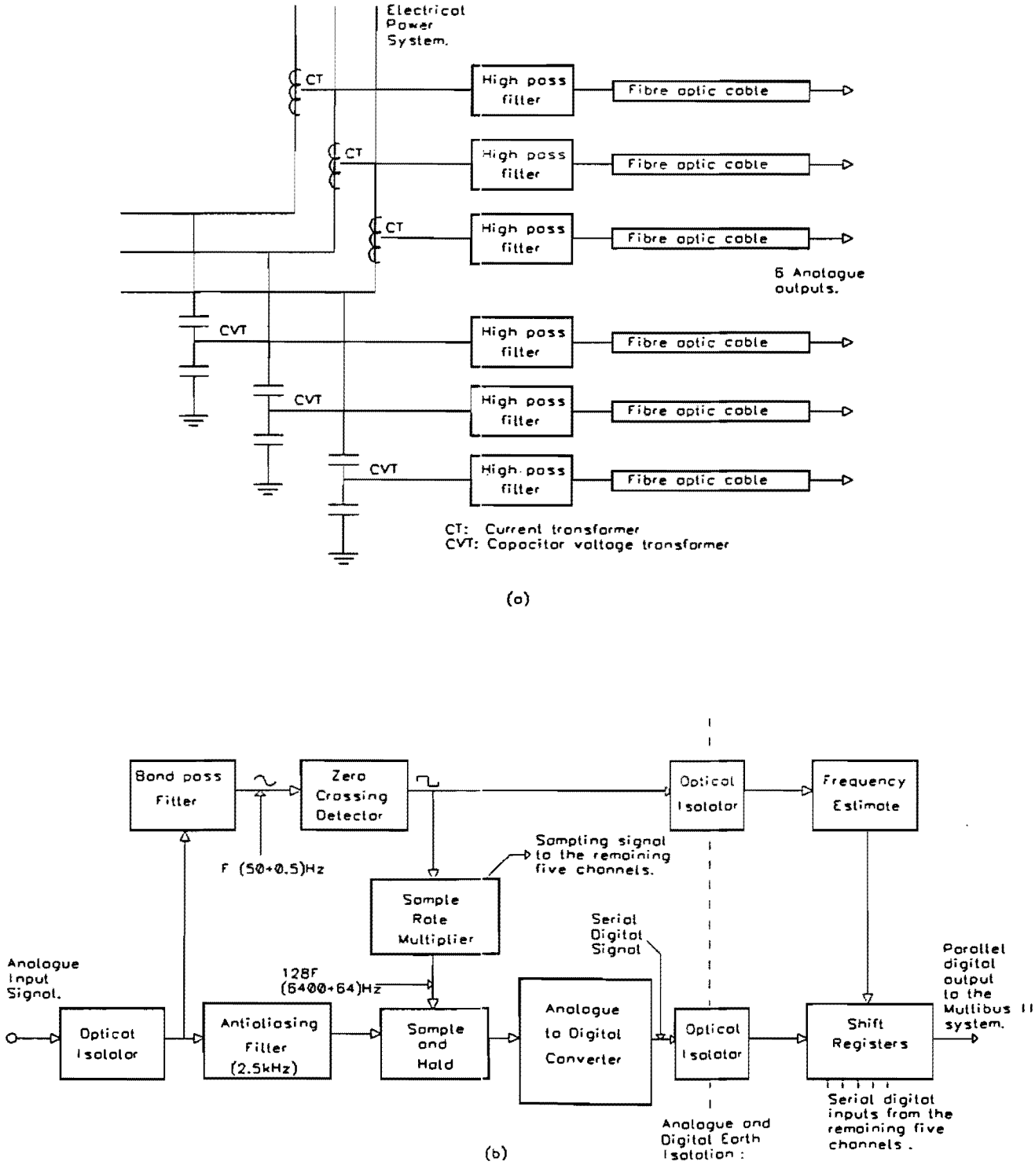

Figure 2: (a) Electricorp interface and signal conditioning equipment. (b) One channel of the data acquisition firmware.

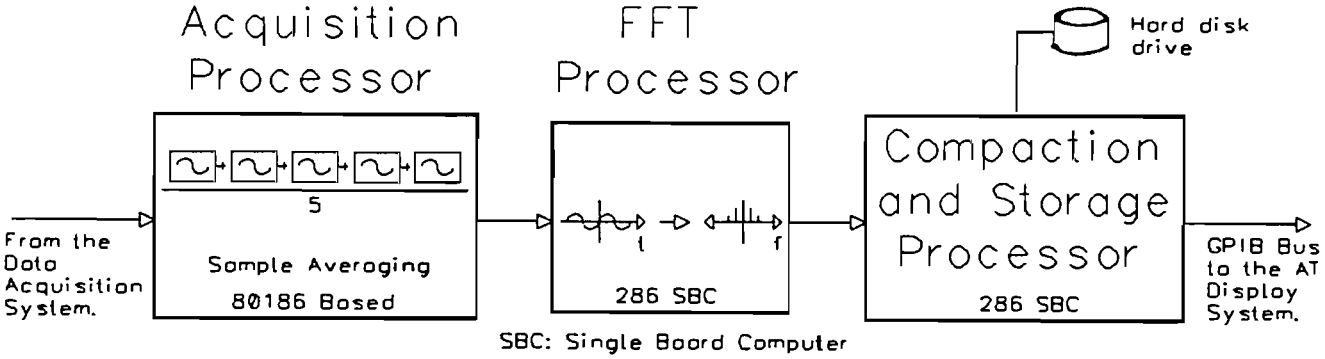

Figure 3: The three main functions performed by the Multibus II system boards.

The sampling signal is produced by the ***sample rate multiplier***. This device combines an 8751 micro-controller, and a high speed counter (operating at 22MHz), to produce 128 pulses, uniformly spaced in time, within one period of the fundamental (which is continuously changing in frequency). The first sample pulse is locked to the zero crossing of the fundamental waveform. Hence a rectangular window is effectively applied over one period of the fundamental, almost completely eliminating the problem of spectral leakage [5][6][7].

The output of the analogue to digital converter is a serial digital signal, which is converted to a parallel form by the shift registers shown in Figure 2(b). The data acquisition system also performs an estimate of the fundamental frequency, and sends this, along with the parallel digital data, to the Multibus II system, discussed in the following subsection.

2.2 The Multibus II system

A system which provides a parallel processing environment, such as the Multibus II system, facilitates the refinement of the processing requirements of this problem into three main parts, with each part performed by an autonomous single board computer, as illustrated in Figure 3.

2.2.1 The Acquisition Processor

Data from the data acquisition firmware system are passed directly to the memory of the first board in the Multibus II system - the acquisition processor board. This is a stand alone board (it does not run any operating system) and is based on an 80186 microprocessor.

Each of the six channels of time domain data is averaged over five consecutive cycles of the fundamental component. This reduces the 'picket fence effect'[3] by narrowing the frequency bins centred on each harmonic.

Alternatively, the picket fence effect can be reduced by broadening the time domain truncation interval (by sampling over five periods of the fundamental for instance), which effectively narrows the harmonic frequency bins (the time scaling property of the Fourier transform [5]). This would, however, involve the processing of significantly more data, which is perhaps the major limitation of our instrument at present. Sampling over 5 cycles, instead of one, increases the frequency resolution of the monitor, transforming it from the desired harmonic analyser into a more general spectrum analyser. Resolving frequencies between harmonics is seen as a waste of processing power in this application.

The averaged data are formed into packets, which are queued by the acquisition processor, ready for message passing to the FFT processor.

[3]The process of taking the DFT is equivalent to filtering the time domain signal through a series of bandpass filters, each centred on an harmonic. Because the DFT operates on a finite set of data, the filter characteristic is non-ideal, and a signal that is not an harmonic frequency (such as ripple injection) will be seen by the filters (but at a reduced level). So it is possible for signals that are not harmonics frequencies, to interfere with harmonic frequencies in the DFT results.

2.2.2 The FFT Processor

Based on an 80286 microprocessor, this stand alone board uses a radix-2 FFT algorithm to compute the DFT of the averaged time domain data. The requirement that the data be processed in real time restricts the capability of this board from processing six channels of data to only two. However, the capability of the system can be increased from two channels to six by replacing the existing 80286 based FFT board with an 80386 microprocessor based single board computer.

The output data packets from the FFT algorithm are queued ready for message passing to the compaction and storage board.

2.2.3 The Compaction and Storage Processor

To enable the inspection of harmonic levels at a later time, or at a location other than the field, the harmonic data are compacted and stored on a 40Mb Winchester hard disk drive. At present, the only means of compaction is to simply store every 10th or 100th FFT packet, as specified by the user, although numerous other successful compaction algorithms have been designed and implemented as experiments. A time stamp is appended to every FFT packet, enabling the accurate replay of a period of time. The storage and replay abilities have not been implemented yet. The eventual aim is to incorporate an event triggered recording ability into the system. At the instant an event occurs, the instrument begins recording harmonic levels for predefined times preceeding and following the event. An event might be characterised by a certain harmonic level exceeding the legal limit, although it will eventually be user definable.

In addition to compaction and storage, this board sends data to the PC-AT for display over a GPIB bus, and acts as a base to which other boards report exceptions if and when they occur. These multiple tasks are handled efficiently by the Intel RMX286 real-time multi-tasking operating system running on this board.

2.3 The PC-AT Display System

Perhaps the most important feature of an instrument such as this is the Human interface. The way data are presented to a user is tremendously important to his or her cognition of the results, and the ease with which the system may be configured to perform the desired operations ultimately determines its popularity, and is conducive to its correct use.

The user interface to this instrument is mouse driven and uses icons (graphically drawn keys) to provide a very comprehendable instrument interface.

Data are displayed on graphs of harmonic voltage, current, impedance, and power against harmonic order. Both the magnitude and phase of these quantities can be displayed. Each graph is contained on a separate window, and the windowing system enables a user to layout the display to suit his or her particular requirements. This is achieved by enabling a user to move a window about on the display, shrink or enlarge it, and to completely remove it.

In addition to the aforementioned graphs, the absolute fundamental frequency is shown on the display, and an indication of whether or not it is within the limits for harmonic monitoring is also shown.

3 CONCLUSION

A Multibus II multiprocessing computer system provides an environment suitable for real time analysis and monitoring of harmonics.

Upon completion of a six channel harmonic monitor, the instrument should be calibrated - to account for phase errors introduced by analogue devices such as transducers and anti-aliasing filters. The monitor can then be used to verify results obtained from harmonic simulations performed in the laboratory, and to assess compliance of electricity consumers to harmonic legislation.

ACKNOWLEDGEMENT

The authors are grateful of the financial support offered by the Electricity Corporation of New Zealand and the Power Systems Group of the Electrical Engineering Department for the development of this instrument. A.J.V. Miller acknowledges the award of a University Grants Committee postgraduate scholarship, and we thank Professor J. Arrillaga for his interest in this project.

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